High precision time measurement electronics for MRPC

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Content

- Readout scheme for MRPC
- Prototype design of readout electronics for MRPC
  - Estimation and simulation
  - Design of the pre-amplifier
  - Design of the high speed waveform digitizer
- Performance testing

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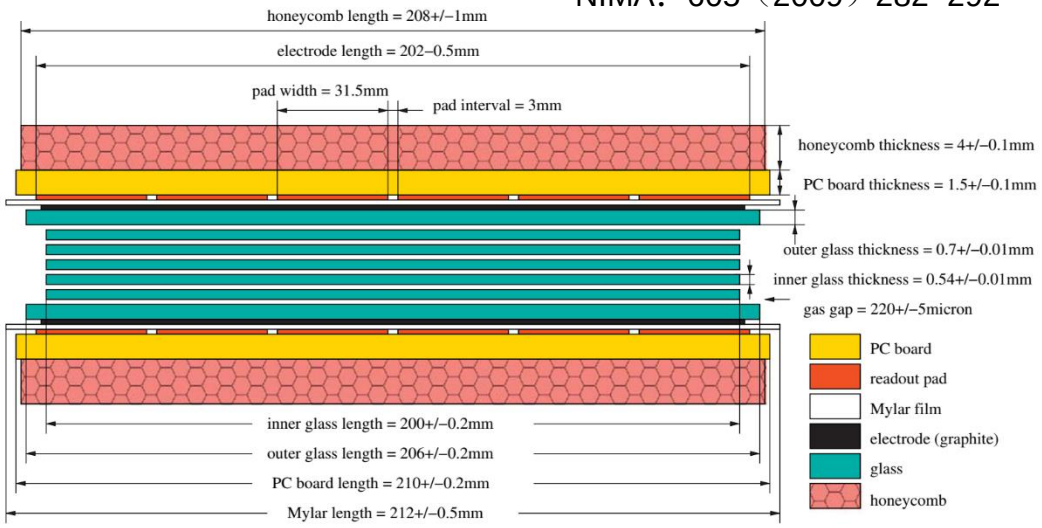
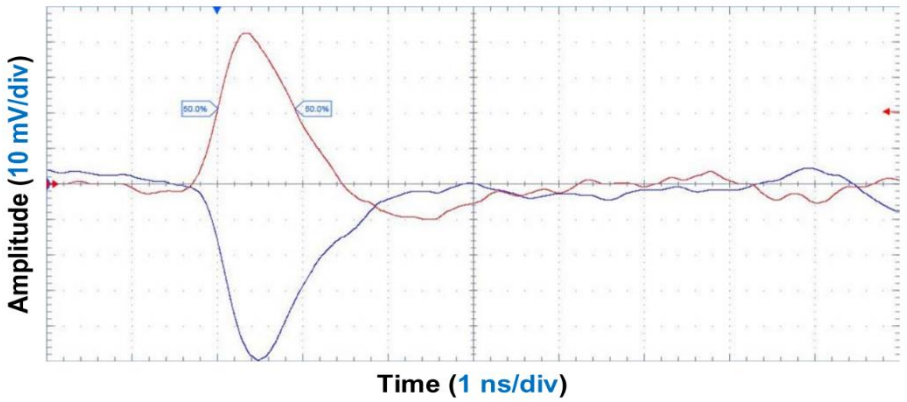
MRPC Detector & Output signal

- MRPC features high time precision
- Next generation:

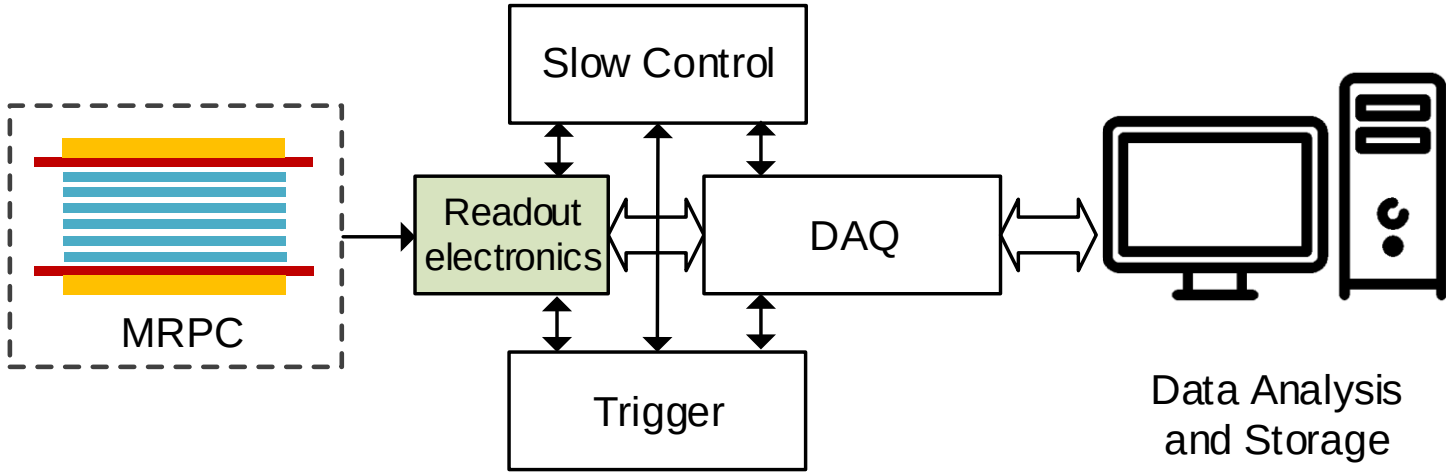
  enhanced from 60~70 ps to 20~ 30 ps
- Output signal:
  - High speed, rise edge <1 ns
  - Small amplitude: < 10 mV @ 50 Ω

NIMA：605（2009）282~292





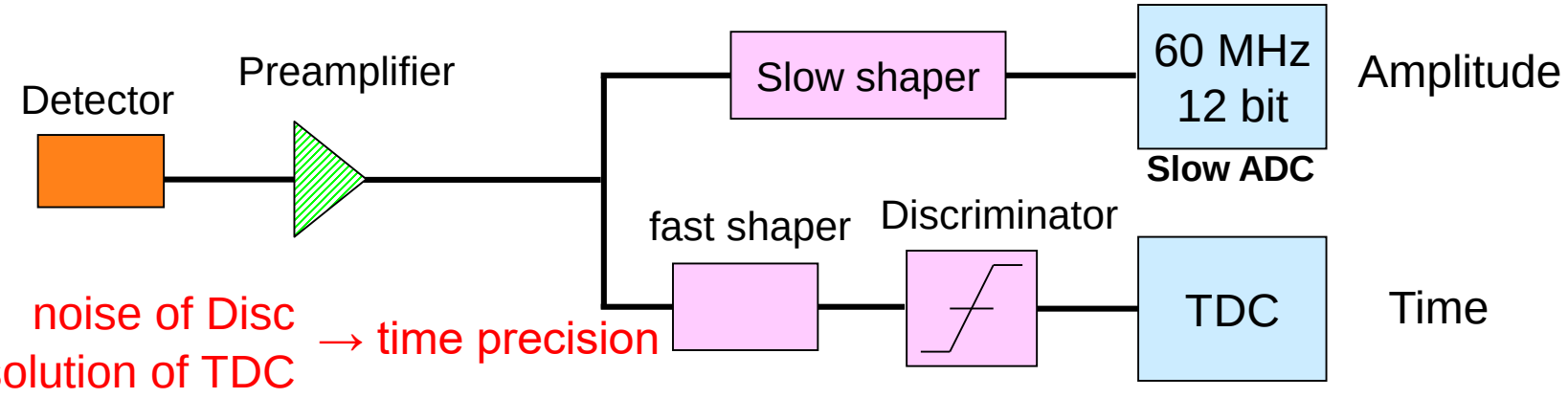
Readout electronics for MRPC



- Requirement on the electronics:
  - High measurement precision: time resolution of 10~15 ps
  - High bandwidth of the front end electronics: >500 MHz
  - Low noise: the signal amplitude < 10 mV
  - Integrating multi channels within one module.

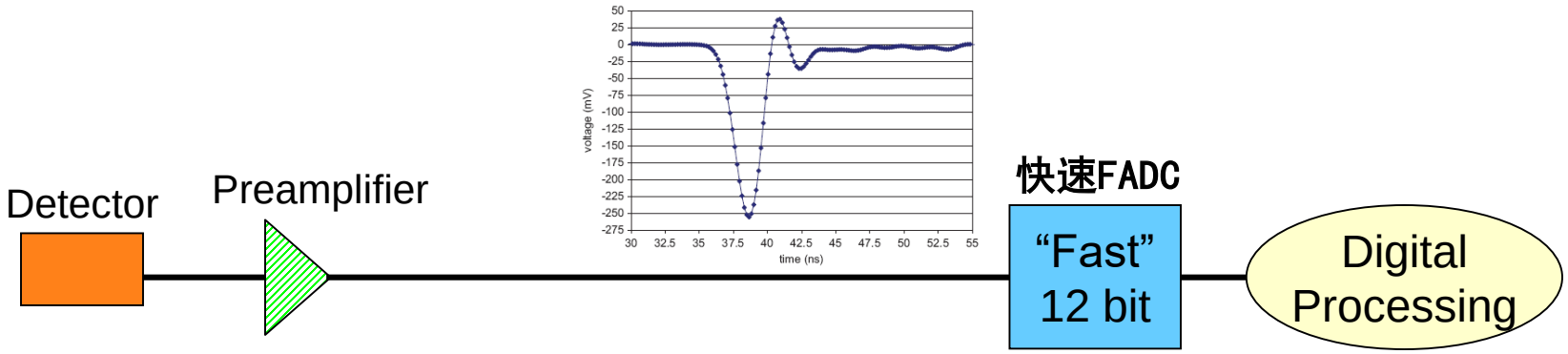
Two methods for time measurement

Method 1: Time discrimination + TDC (Time-to-Digital Converter)



noise of Disc
resolution of TDC → time precision

Method 2: Waveform digitization + Digital processing



Flash ADC → Power consumption, density, cost

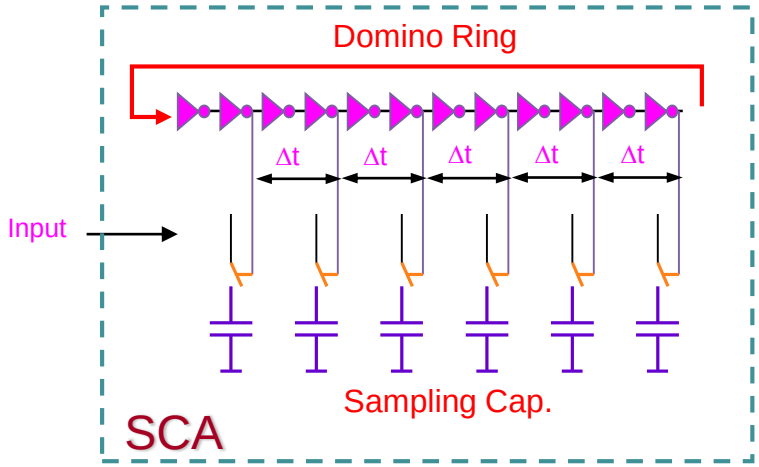
→ Switched Capacitor Array (SCA)

SCA based waveform digitization

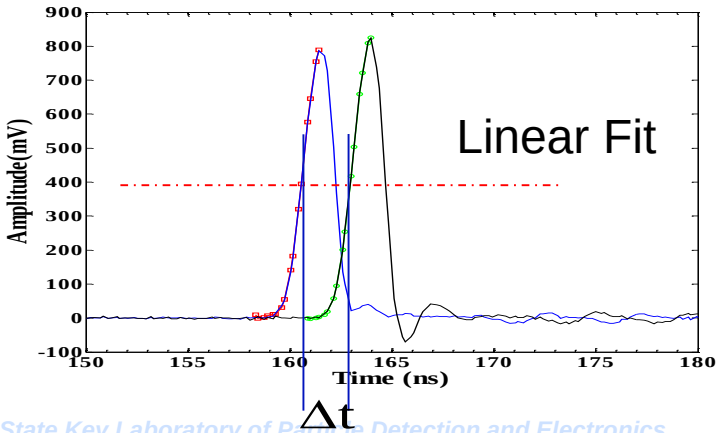
High speed analog transient signal sampling & storage ＋ ADC （SCA + ADC）

high speed sampling

Slow A/D conversion



＋ ADC



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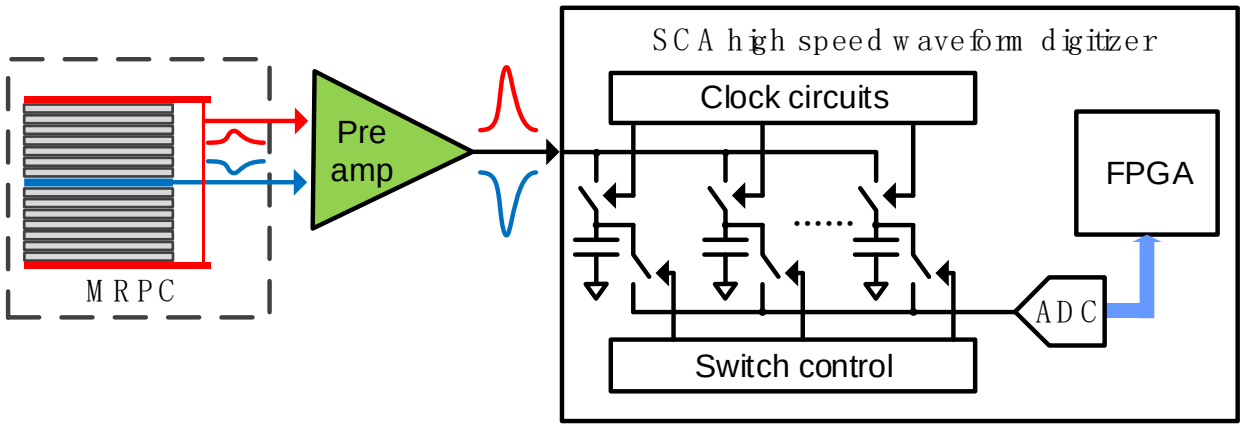
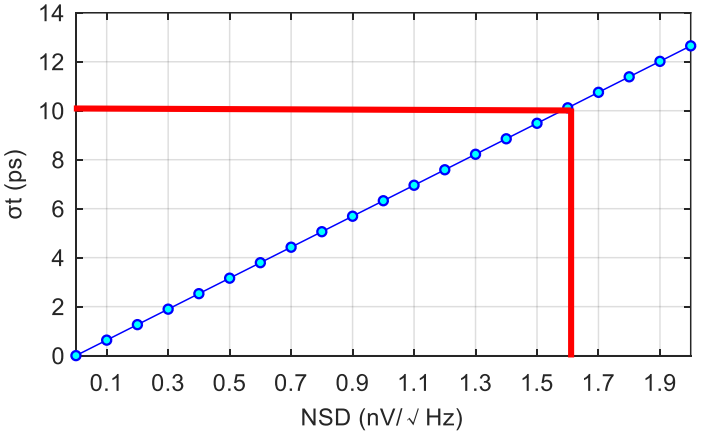
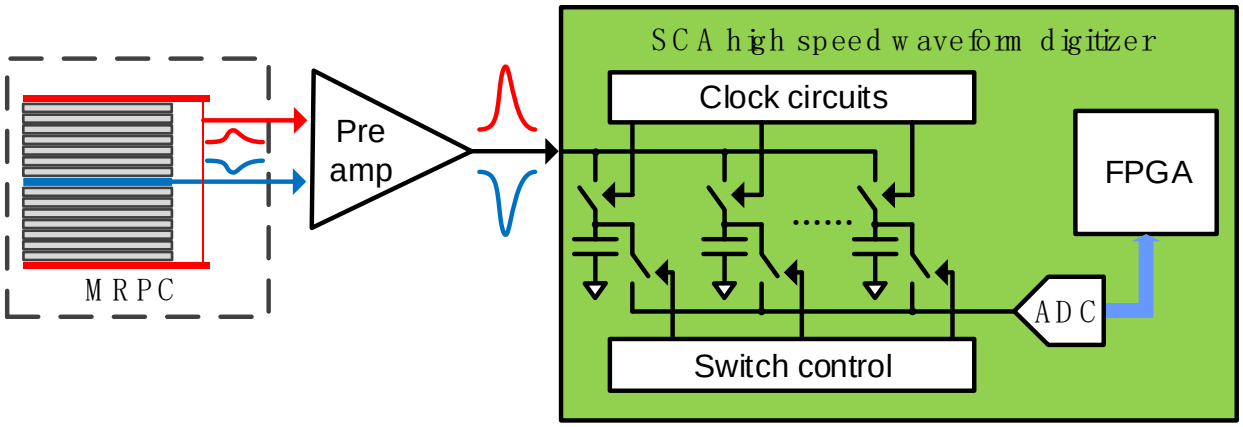
Noise estimation: high speed pre-amplifier



- Key parameters:
  - Bandwidth consideration: 500 MHz~ 1 GHz
  - Signal amplitude: 5 mV → Gain >20
  - Noise Spectral Density (NSD) < 1.5 nV/ √Hz
  - $\sigma_t = \frac{t_r}{A} \times NSD \times \sqrt{BW}$



Noise estimation: waveform digitizer



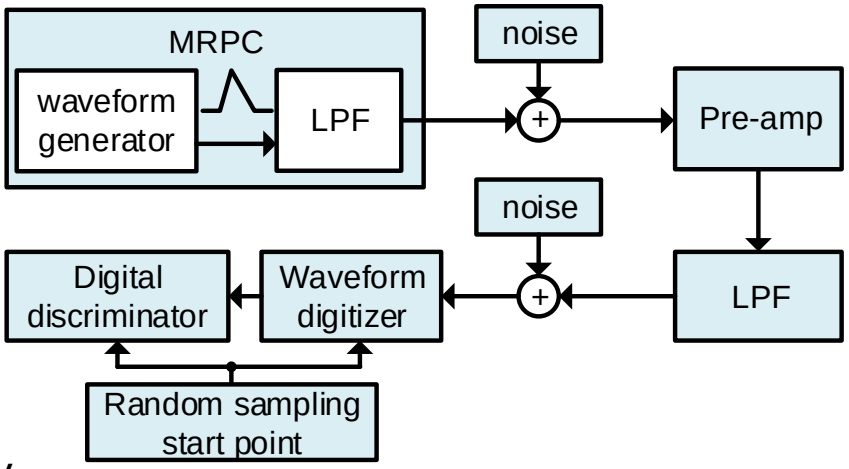
Key parameters:

- $\sigma_t = \frac{\sigma V_i}{A} \times \sqrt{\frac{t_r}{F_s}} = \frac{\sigma V_i}{A} \times \sqrt{\frac{1}{3 \times BW \times F_s}}$
- Bandwidth (cable) → 550 MHz
- Enough samples of the leading edge → sampling rate (Fs): 5 Gsps
- Noise requirement < 1.5 mV

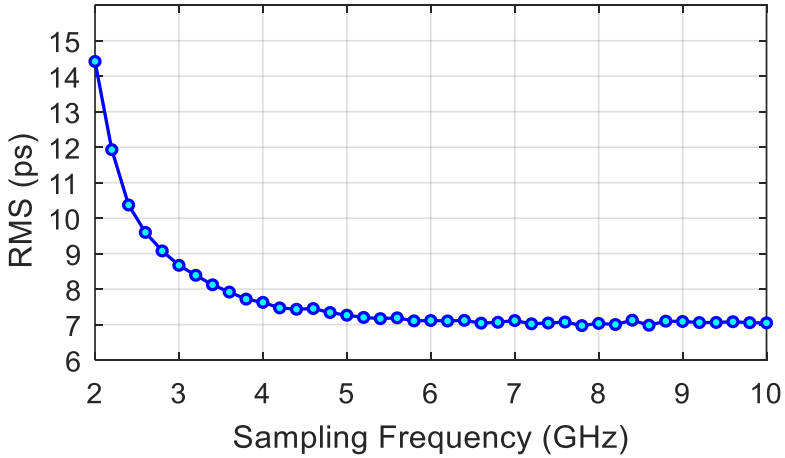
A/mV	σV_i/mV	BW/MHz	F_s/GHz	σ_t/ps
5	1	550	5	70
35	1	550	5	10
53	1.5	550	5	10
100	1.5	550	5	5.2

Performance simulation

- Simulation test bench
  - Platform：MATLAB
  - Input signal amplitude：5 mV
  - NSD of pre-amp：1.5 nV/ √Hz
  - Gain：20
  - Noise of the waveform digitizer：1.5 mV



- Simulation results:
  - Time resolution is better than 10 ps @ Fs> 3 Gsps
  - When Fs is beyond 5 Gsps, time resolution is almost stable



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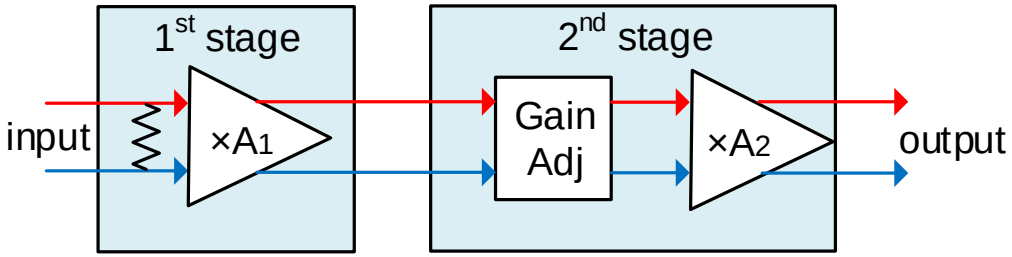
Prototype of the pre-amplifier

- Friis Equation:

$$\mathrm{F} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_n}$$

F is noise figure, G is the Gain. The noise of the main amplification and its preceding stages dominates the noise performance of the whole circuits.

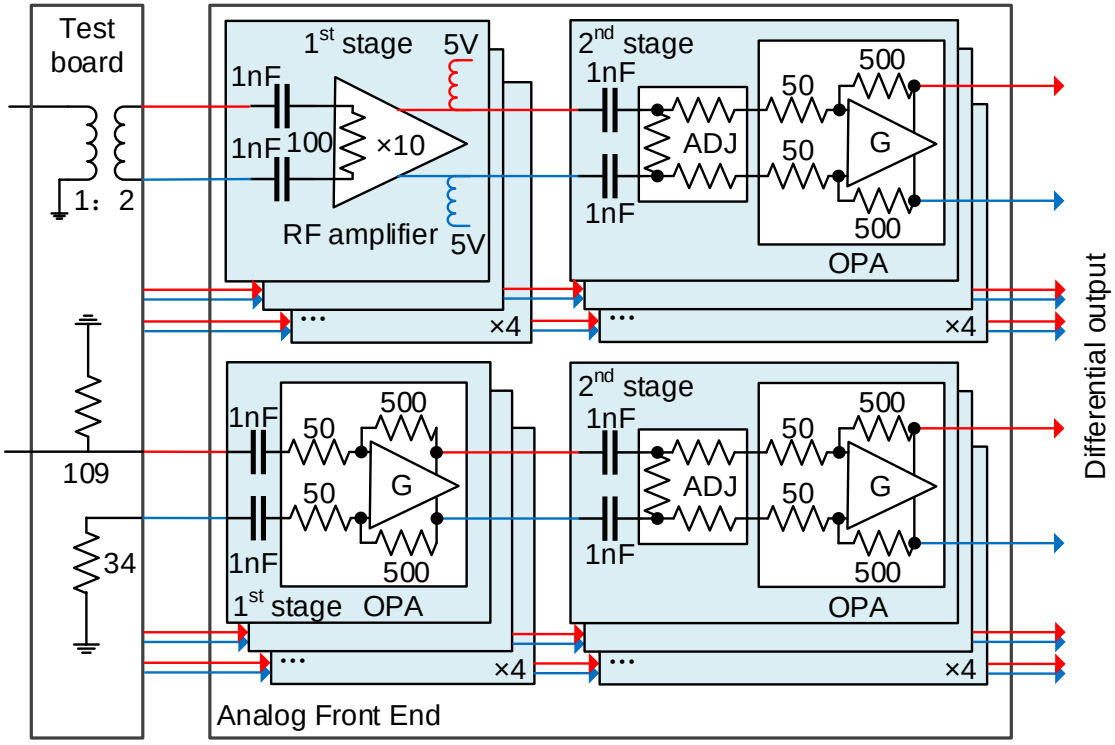
- Circuit scheme:

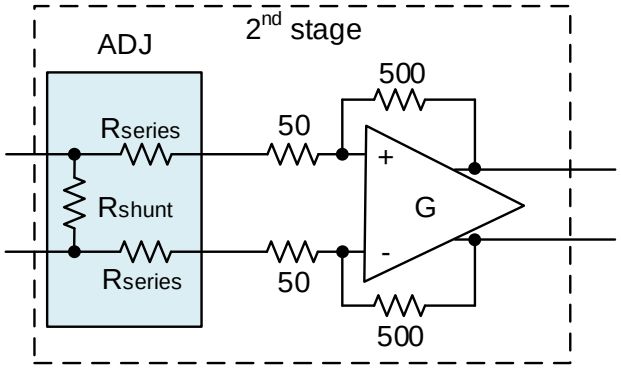


  - Cascading of two amplification stages to achieve a total gain of >20
  - Using high gain, low noise amplifier as the first stage
  - Adding gain adjustment circuit to optimize the amplifier

Prototype of the pre-amplifier

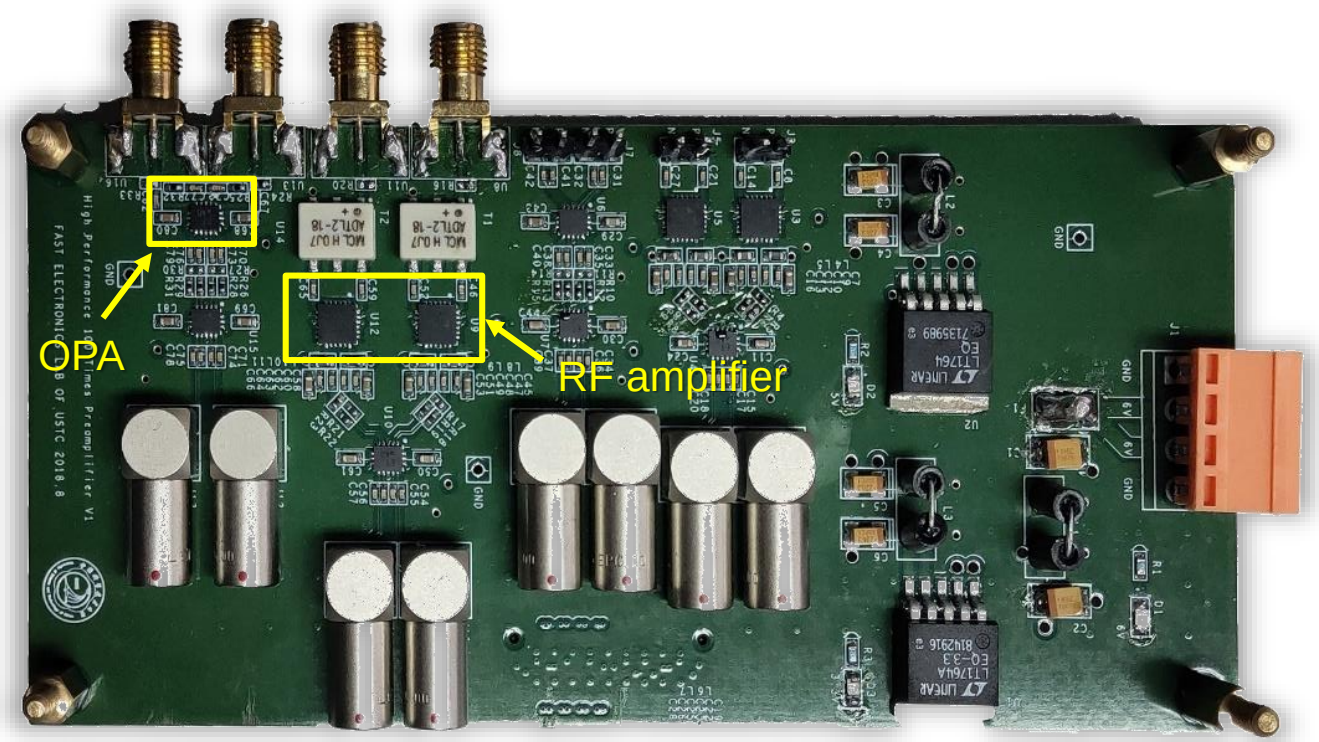
- Two types of amplifiers are used and compared in prototype design.





gain adjustment circuit

Prototype of the pre-amplifier



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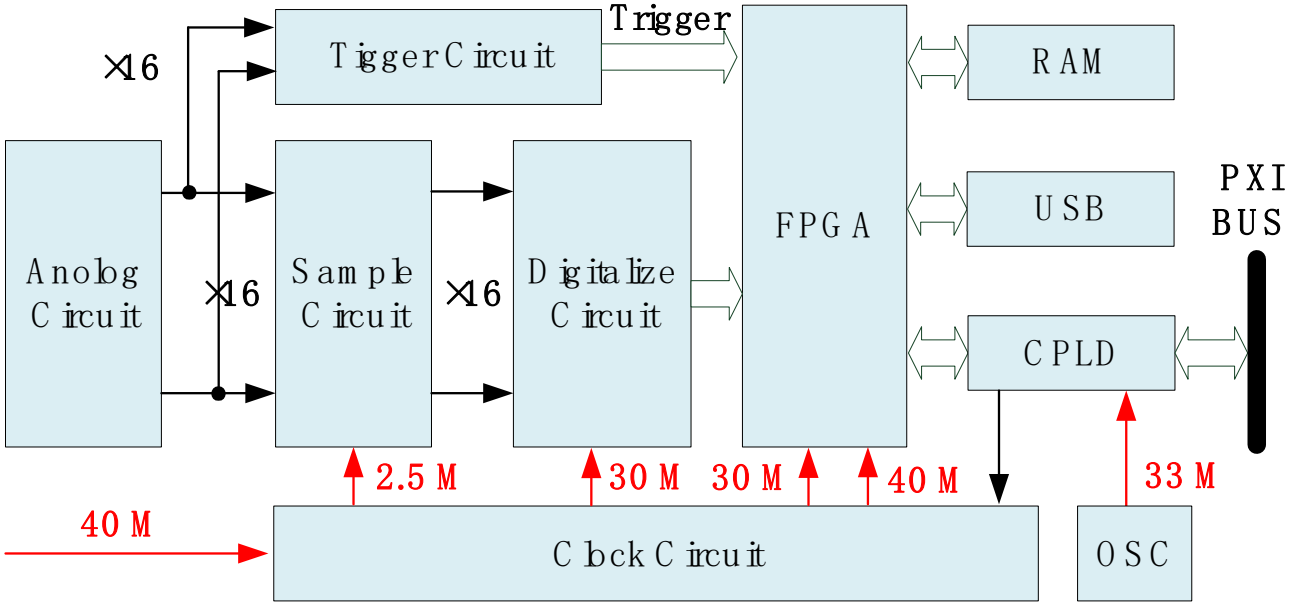
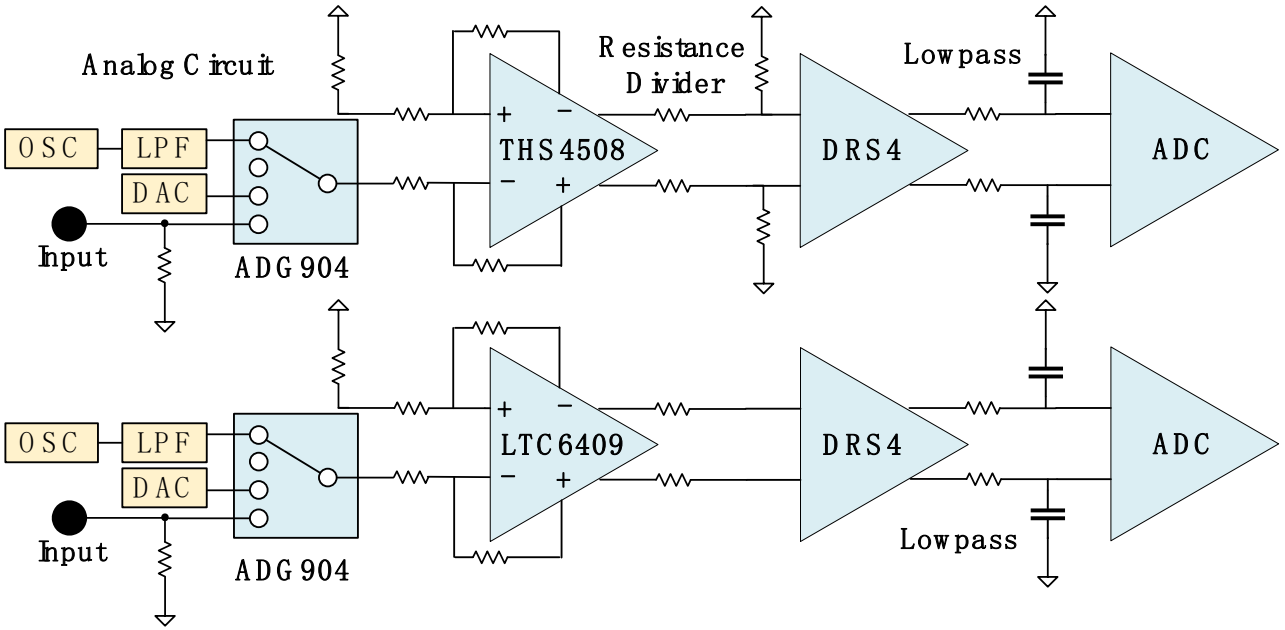
Design of a 16 chl waveform digitizer

- Block diagram:



- 16 channels per module
- Analog circuits: buffering for input signals, calibration signal generation
- Self Trigger Circuits: discrimination, self trigger signal for SCA readout
- Data Readout： USB or PXI interface

Analog Front End of waveform digitizer



- Two amplifiers are employed for comparison
- Using switches to select among:

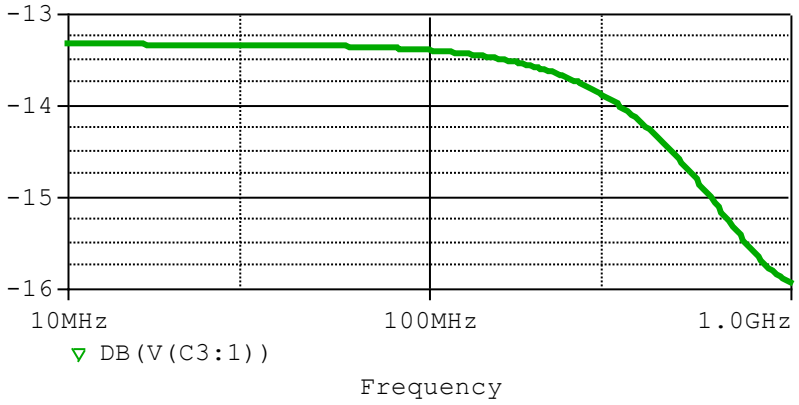
① Analog input signal
② DC voltage from DAC for calibration
③ Sine wave signal for calibration

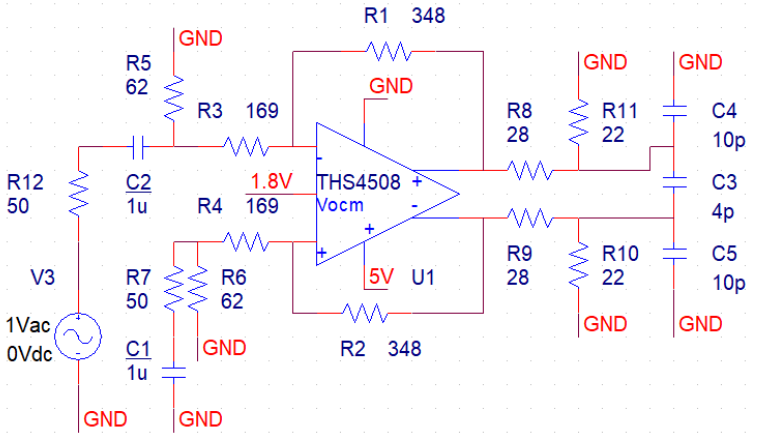
Analog Front End

- Simulation results of bandwidth

Buffer1

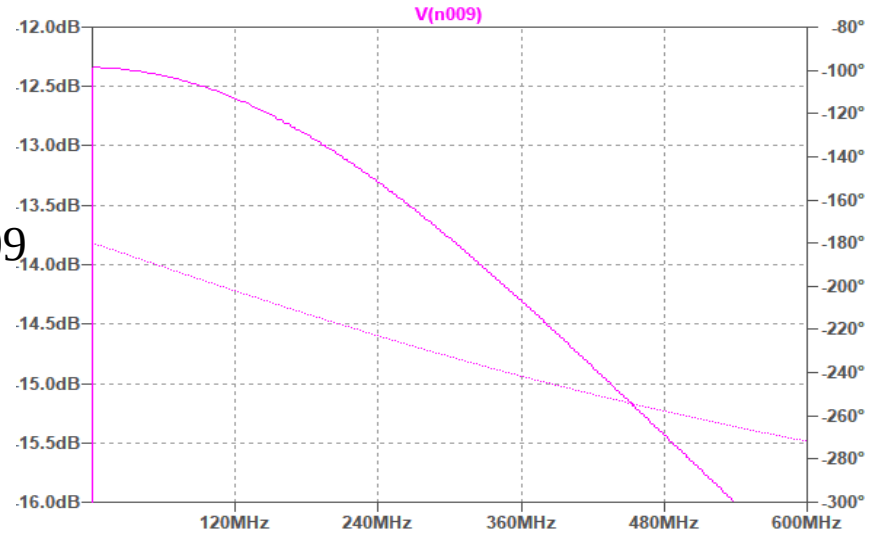
THS4508

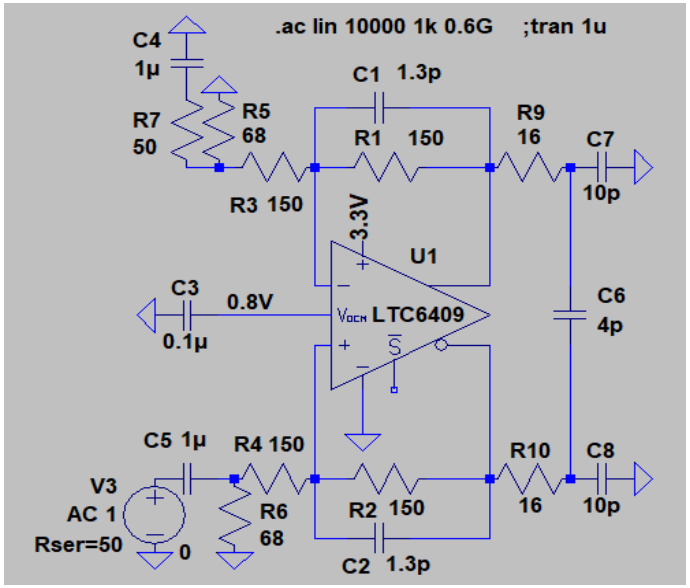




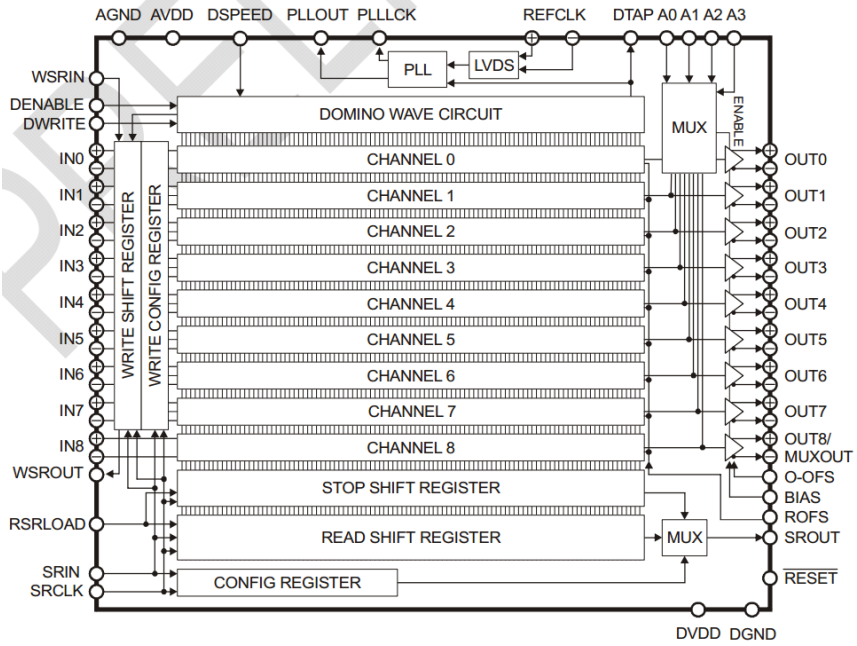
Buffer2

LTC6409



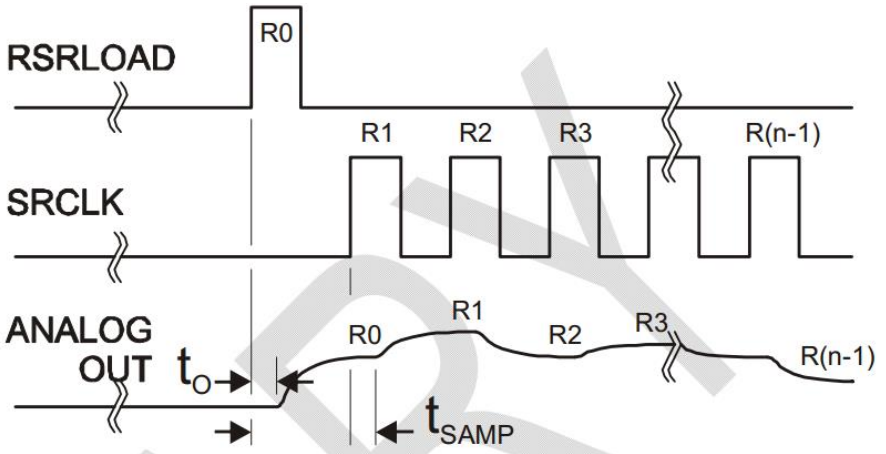


Sampling: SCA – DRS4



Parameter	
Channel no	8+1
-3dB BW	950 MHz
Sampling speed	0.7 Gsps ~ 5Gsps
Readout frequency	30~40 MHz
noise	0.35 mV RMS
Diff input range	< 1 Vpp

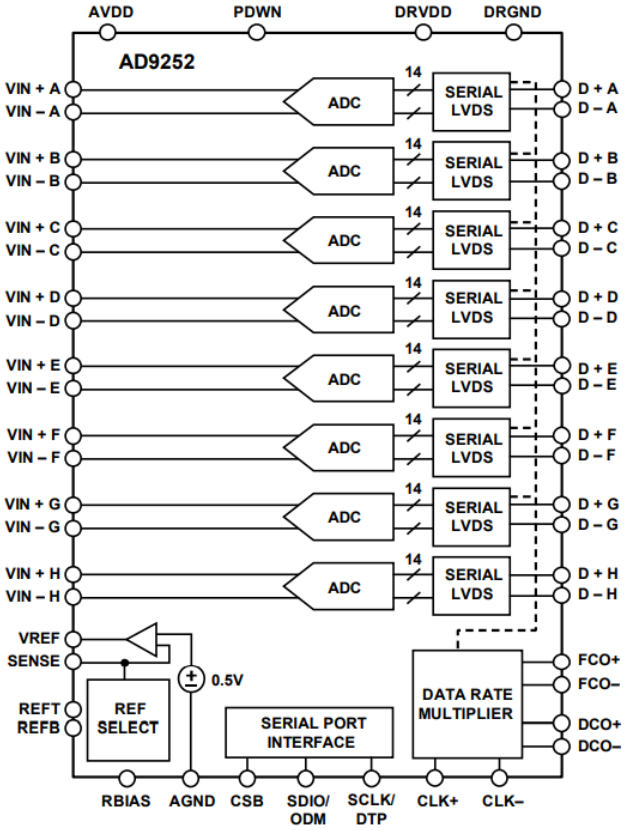
DRS4 output waveform



Quantization

8 chl ADC

AD9252



Parameter	
Channel no	8
-3dB BW	325 MHz
Sampling speed	50 Msps
resolution	14 bits
ENOB	11.8 bits
FSR	< 2 Vpp

ADC output data

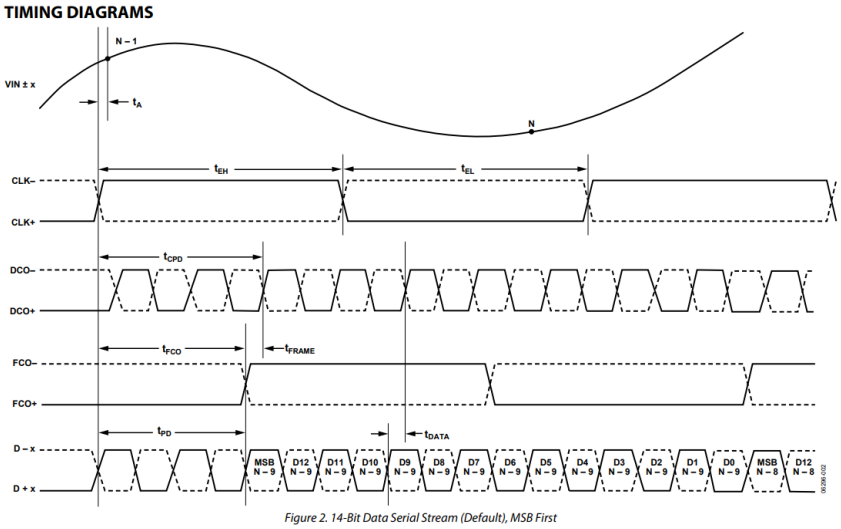
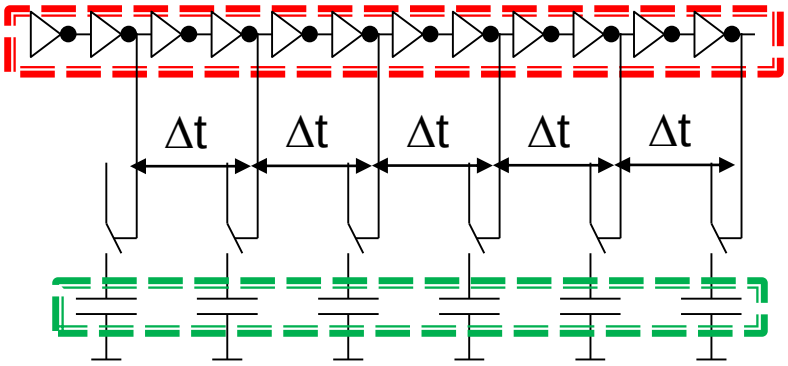


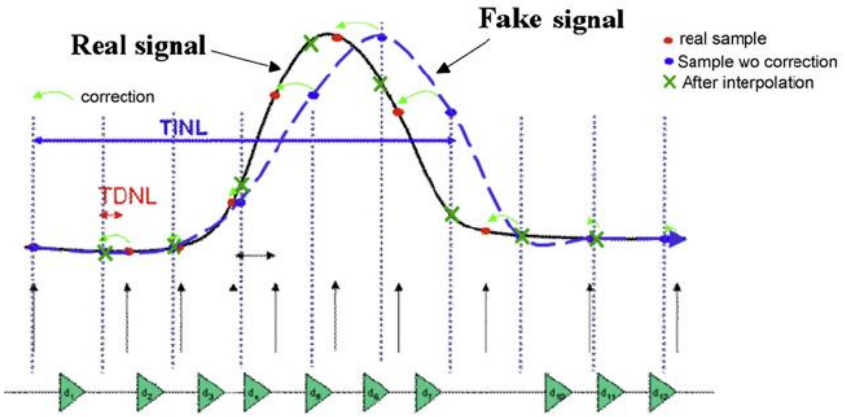
Figure 2. 14-Bit Data Serial Stream (Default), MSB First

Calibration & correction

- (1) DC Offset Variation Error

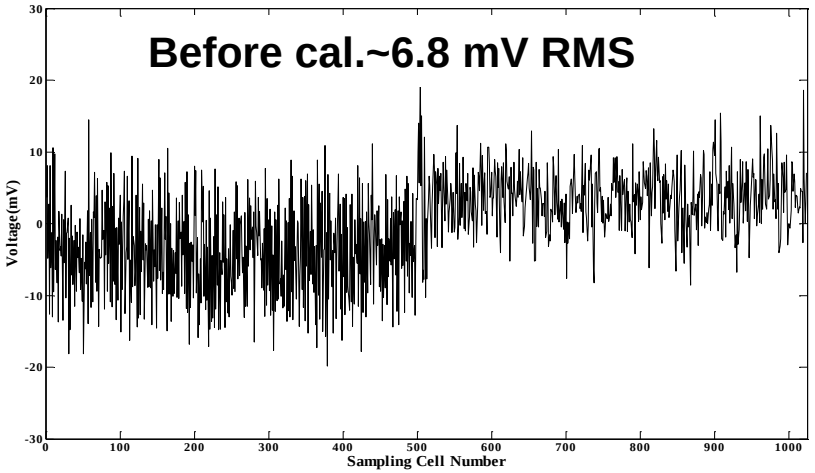


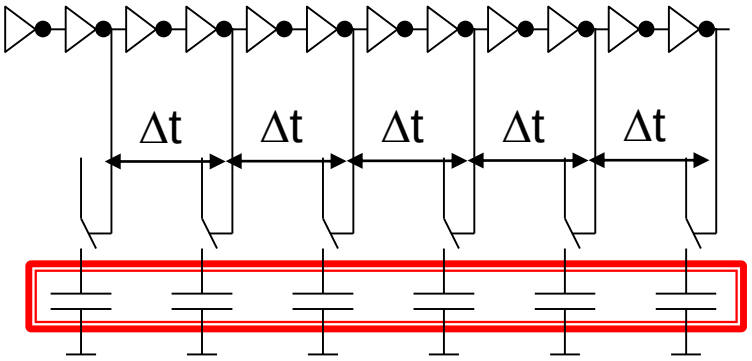
- (2) Uneven Sampling Intervals



NIMA :629 (2011) 123-132

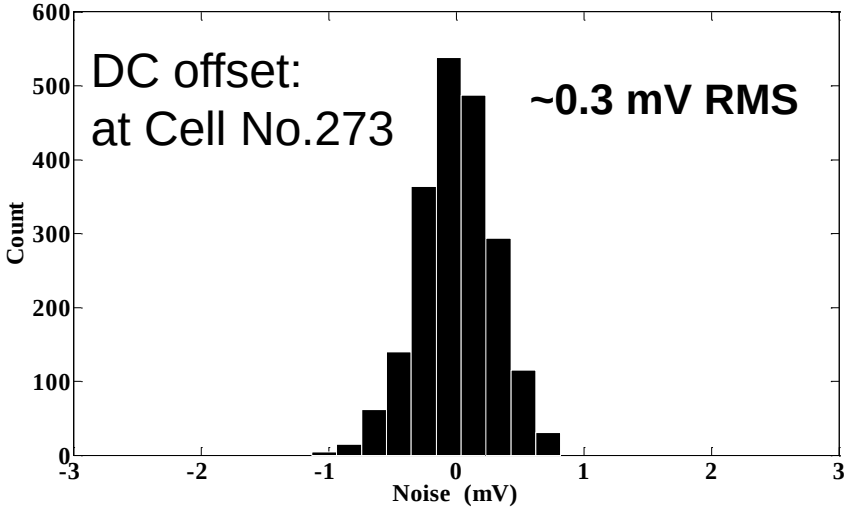
Calibration of DC offset

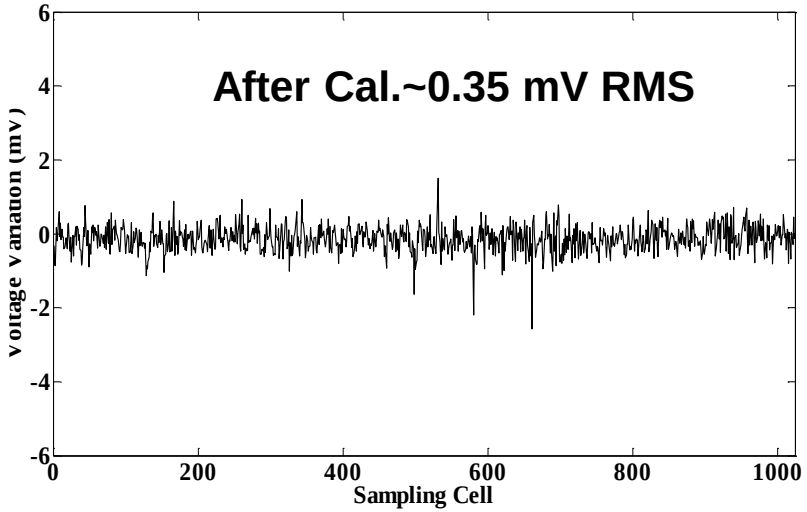




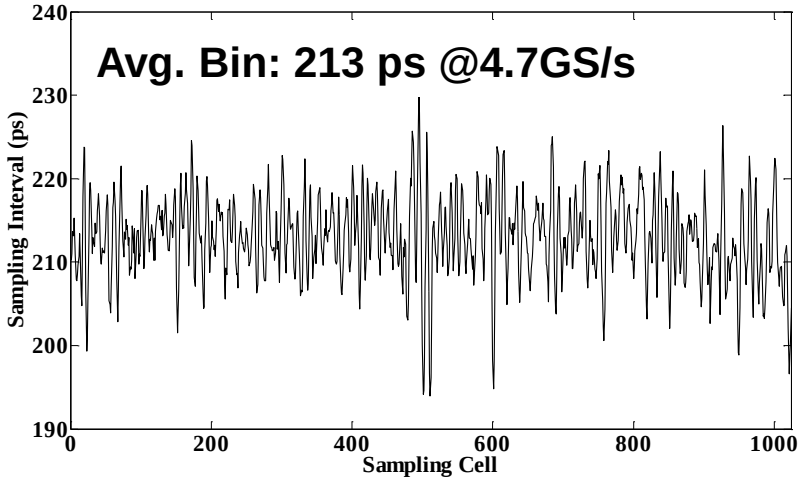
Cell to cell Variation

DC offset: Cell-to-Cell Variation

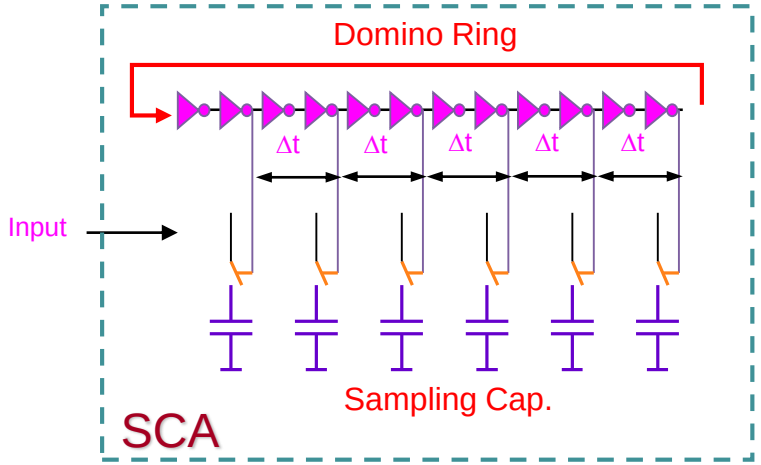


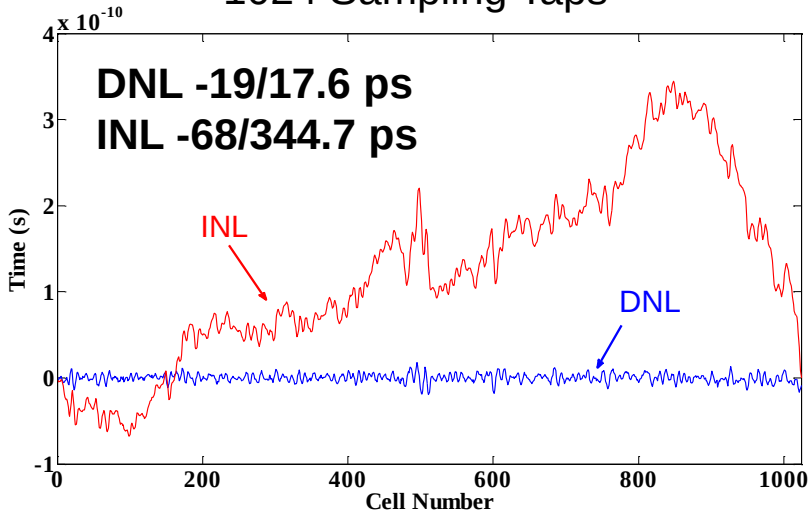


Calibration of Uneven Sampling Interval

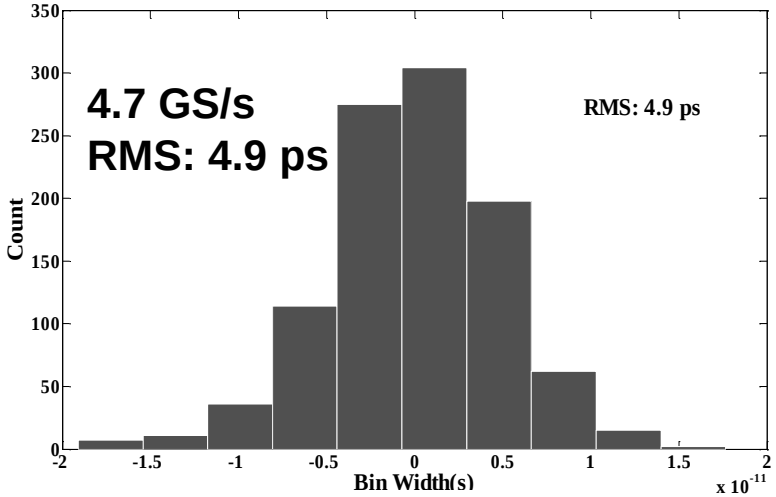


1024 Sampling Taps





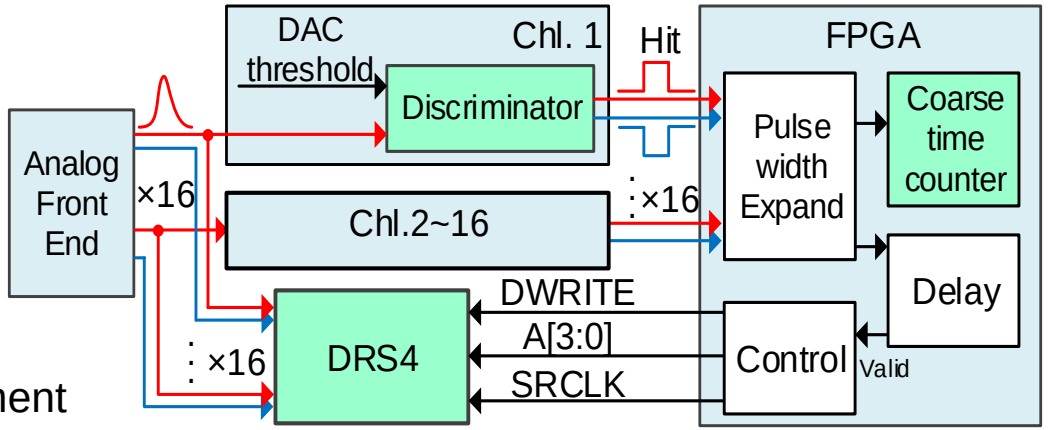
DNL & INL



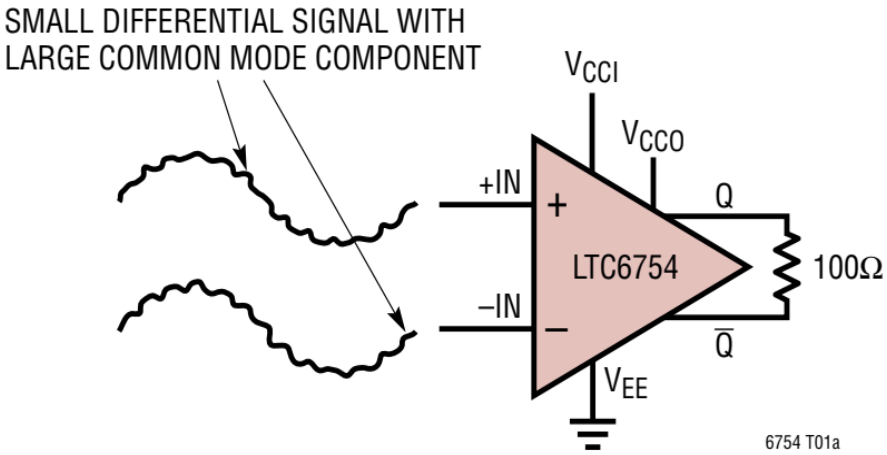
Distribution of Bin width

Time measurement

- Signal process in FPGA
  - Pulse width from disc：1 ns
  - Adjustable delay for readout
  - Based on ROI (Region of Interest)
  - Counter for coarse time measurement

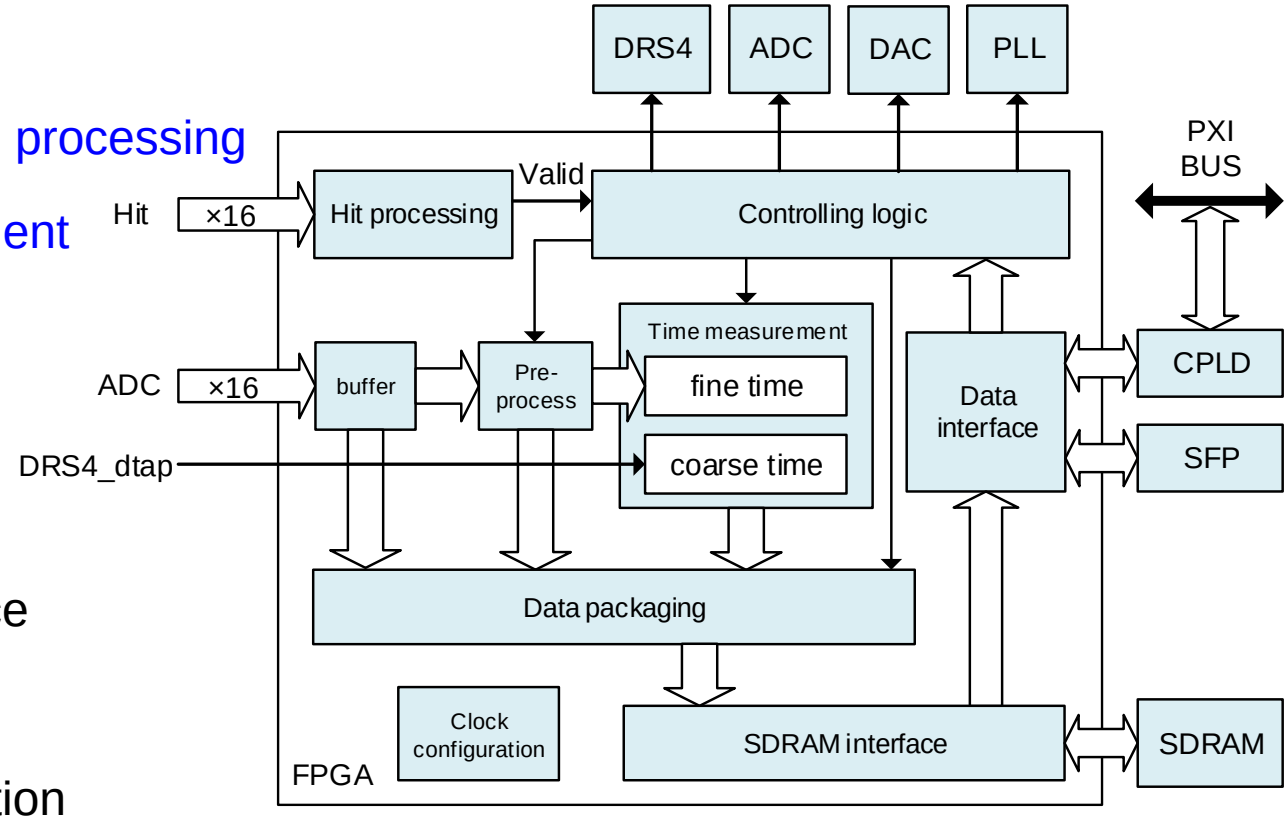


- High speed discriminator：
  - Speed：800 Mbps
  - Delay：1.8 ns



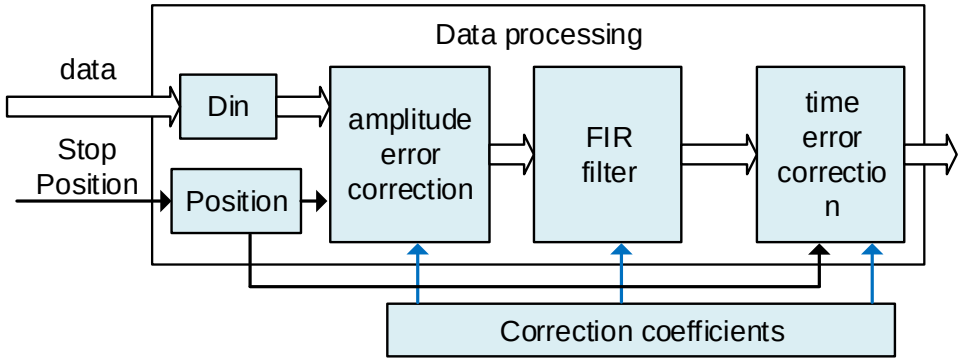
Logic design in FPGA

- Structure
  - buffer
  - Real-time signal processing
  - Time measurement
  - HIT processing
  - Controlling logic
  - Data packaging
  - SDRAM interface
  - Data interface
  - Clock configuration

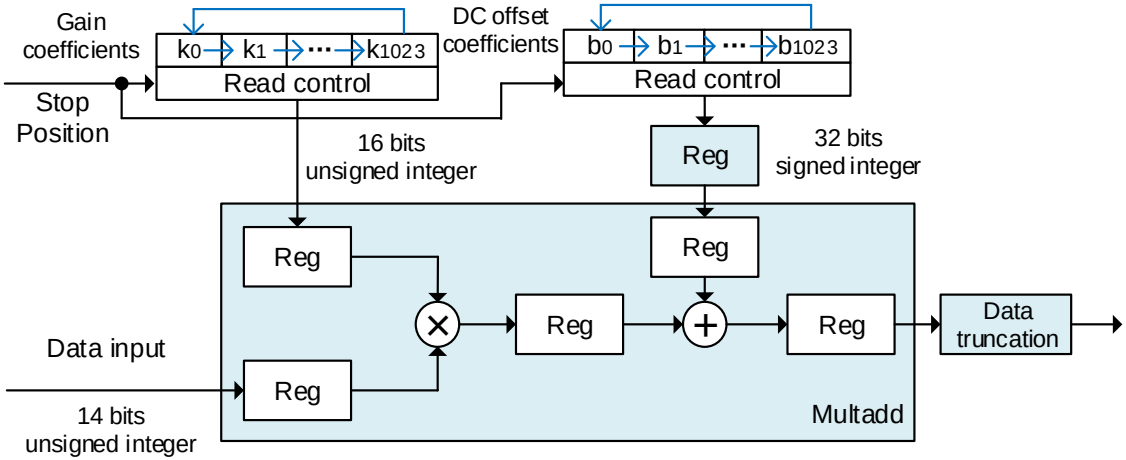


Real-time signal processing

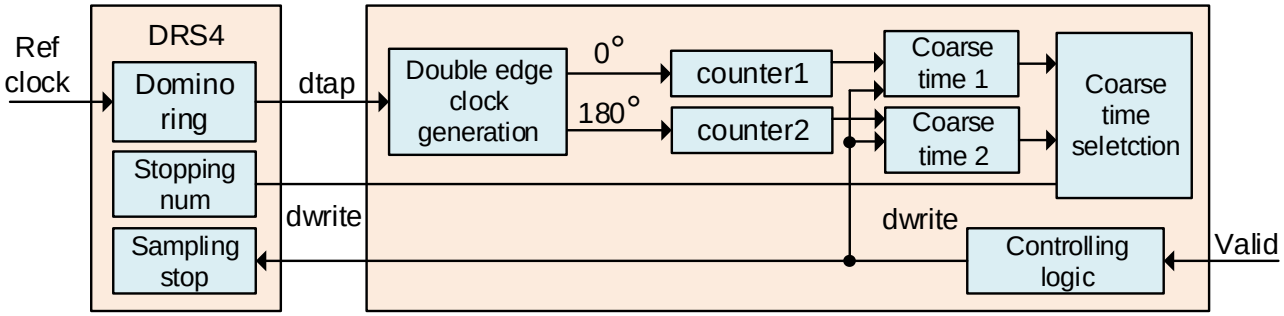
- Signal processing:
  - Amplitude error correction
  - FIR filtering
  - Time error correction



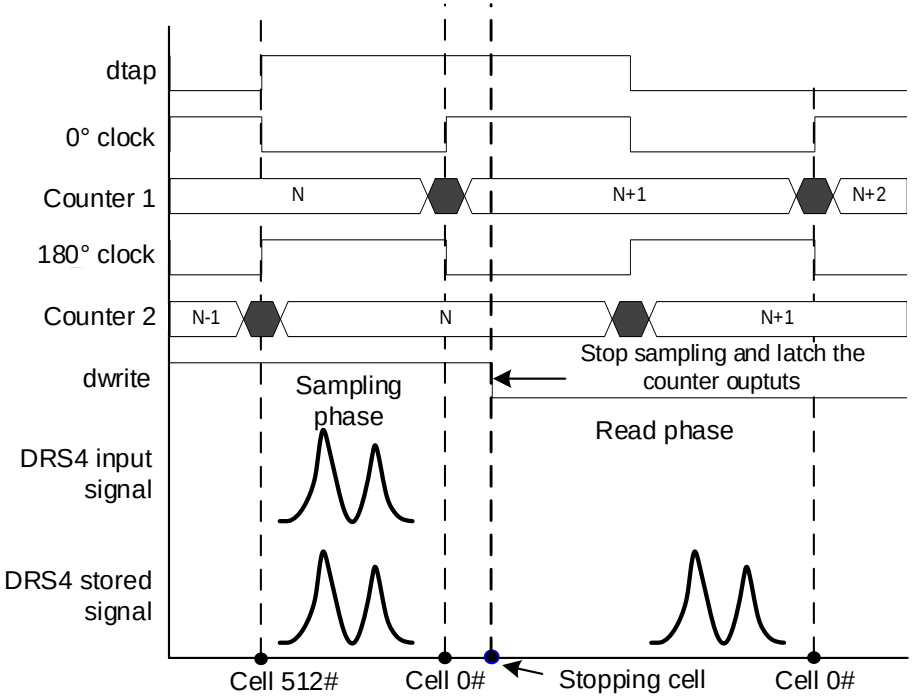
- Amplitude correction
  - Correction coefficients stored in a ring
  - Align the data according to the stop position
  - Processing：Multiplier + Adder



Time measurement

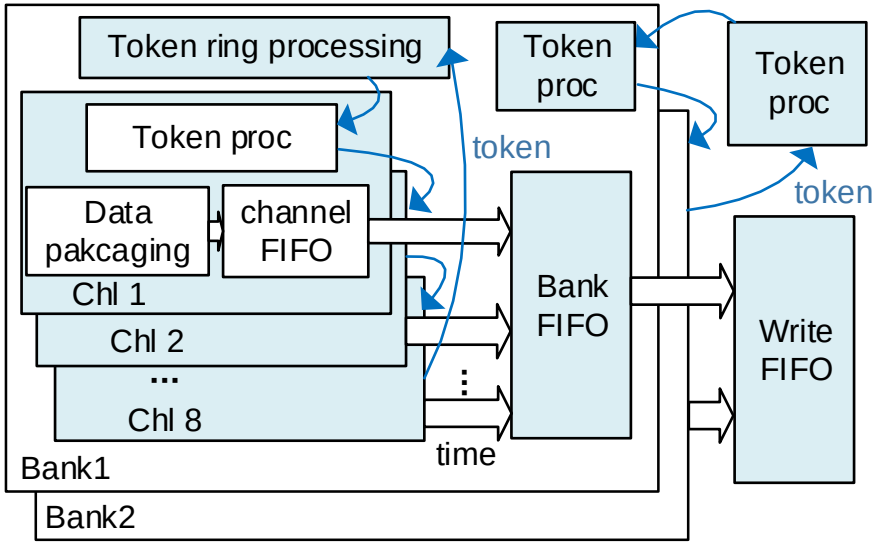


- coarse time measurement logic
  - Counting clock: dtap
  - Double edge counting to avoid meta-stability
  - Counter width: 24 bits，range ~ 3.4s
  - Common counters shared by multiple channels



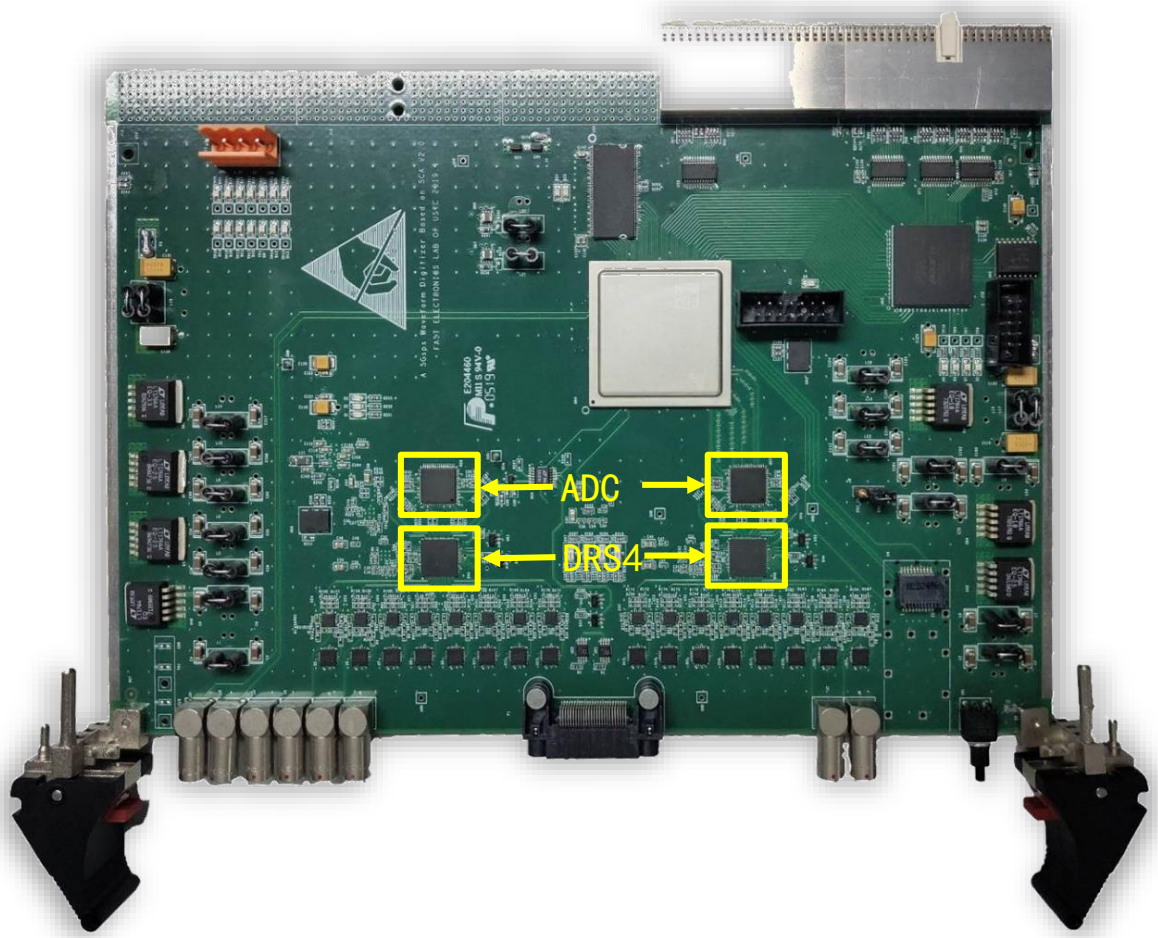
Data packaging and transfer

Header	F0F0
Coarse time [23:12]	12 bit
Coarse time [11:0]	12 bit
Stopping position	10 bit
reserved	C3C3
Digitized waveform	16 bits
……	……
Digitized waveform	16 bits



- Two layers of data buffering based on token ring, to enhance the data transfer efficiency
- When all the data from the FIFO is read out (empty), the token is released to the next channel

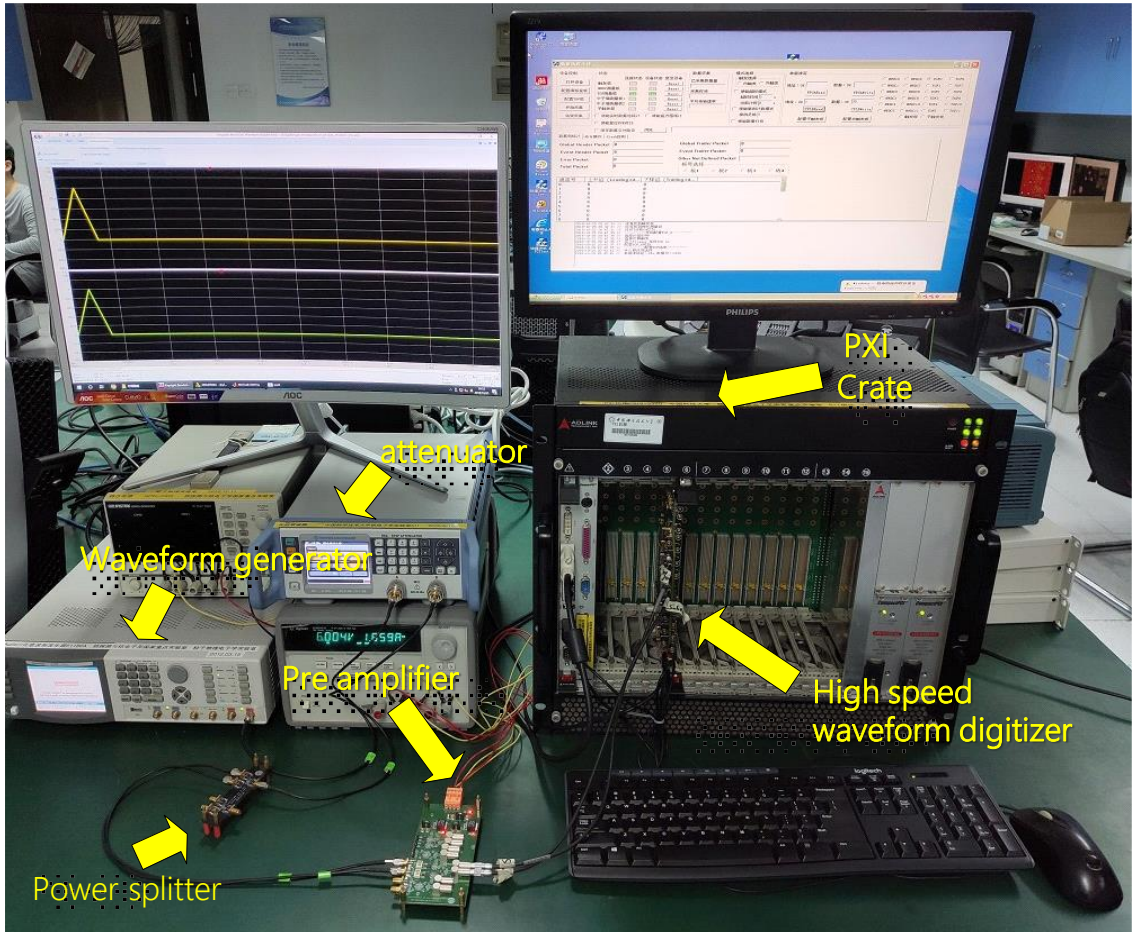
Photograph of the waveform digitizer



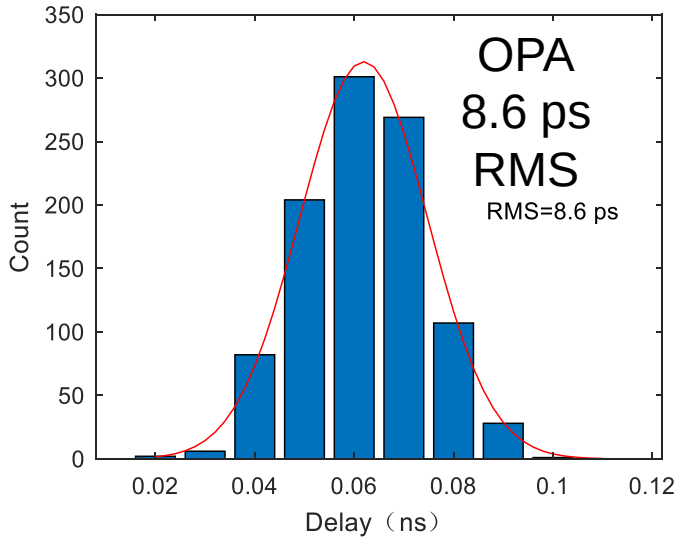
Content

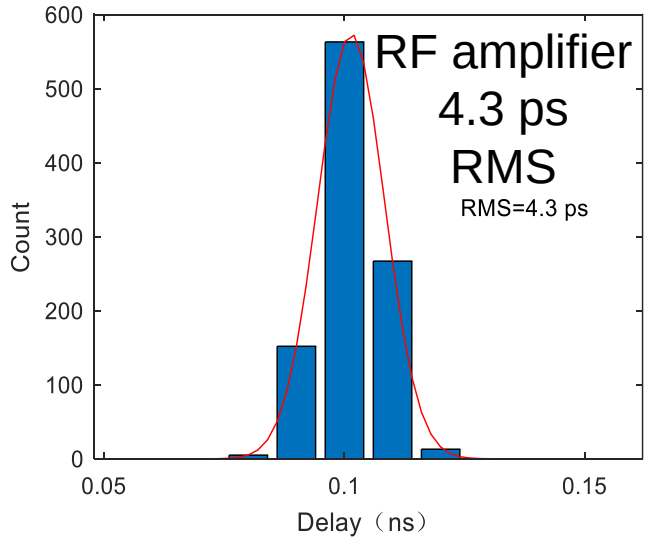
- Readout scheme for MRPC
- Prototype design of readout electronics for MRPC
  - Estimation and simulation
  - Design of the pre-amplifier
  - Design of the high speed waveform digitizer
- Performance testing

Performance testing

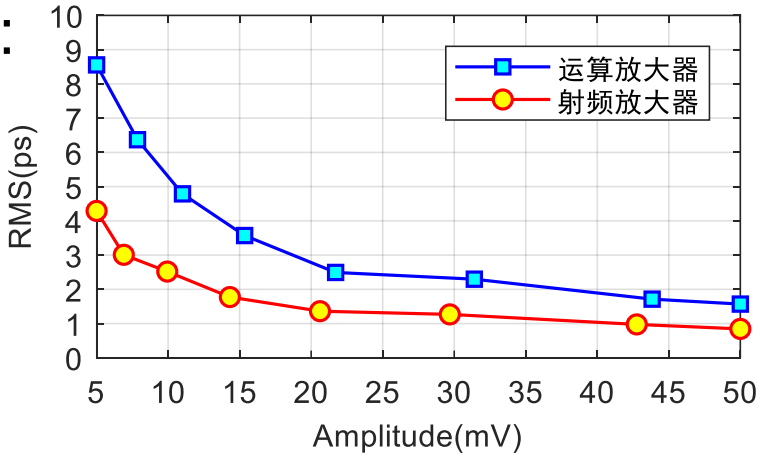


Testing of the pre-amplifier





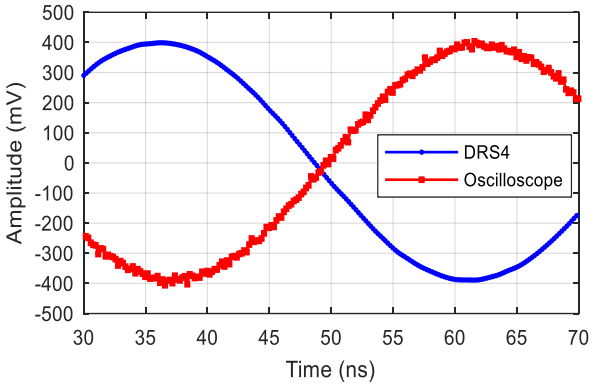
- Time measurement precision:
  - Input amplitude：5 mV
  - OPA:8.6 ps
  - RF amplifier:4.3 ps



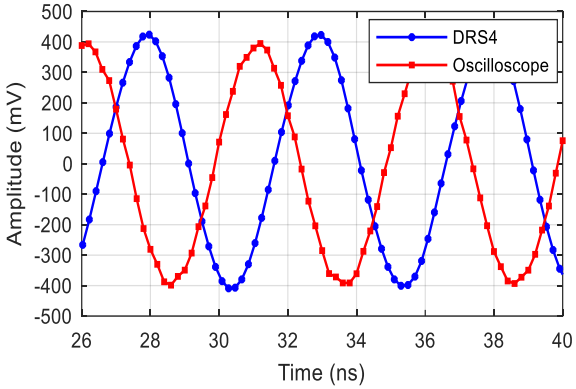
Testing of the waveform digitizer

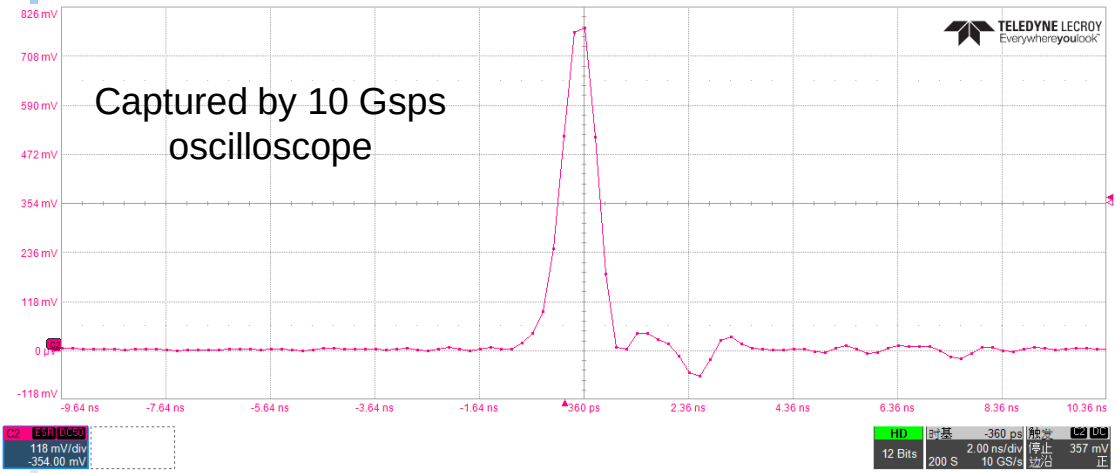
- Transient waveform sampling
  - RF Signal source：
    N5181A
  - Pulse generator：
    81180A

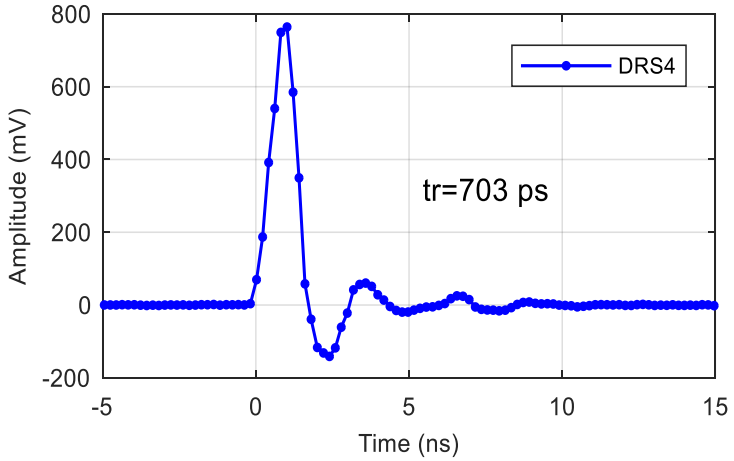
20 MHz



200 MHz

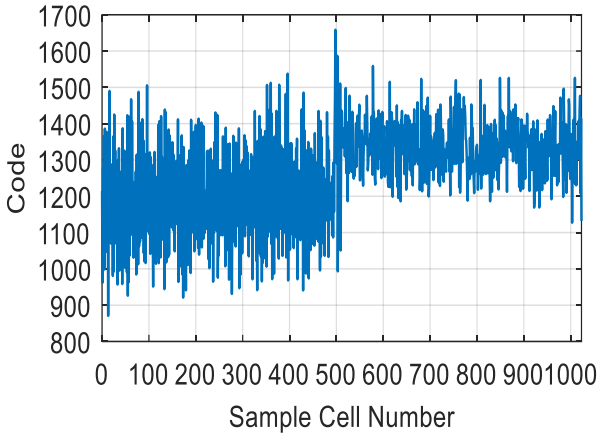


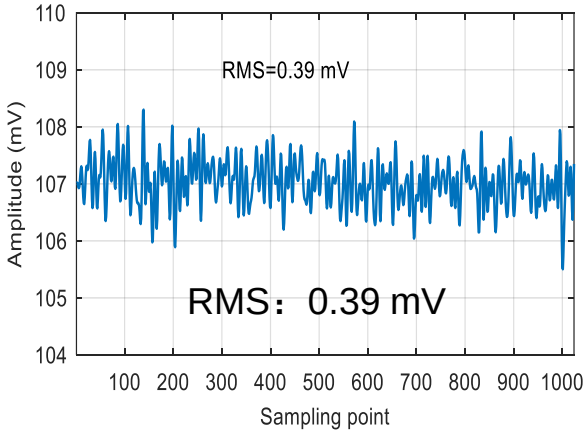




Testing of the waveform digitizer

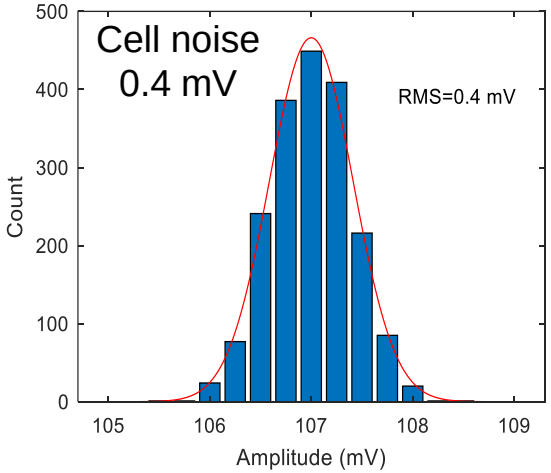
DC voltage sampled results (before correction)

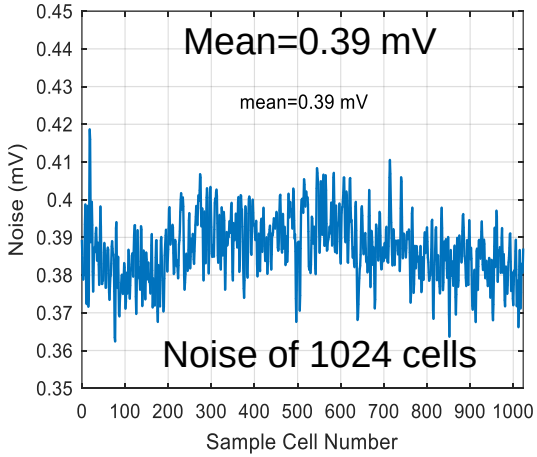




DC voltage sampled results (after correction)

- Noise performance
  - After correction and filtering
  - Averaged noise：0.39 mV

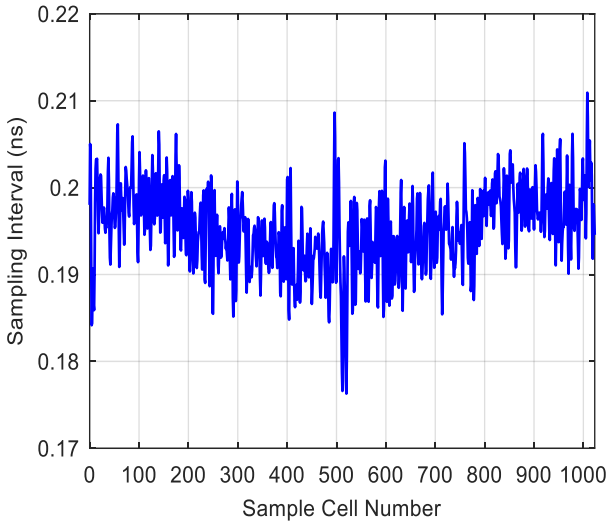


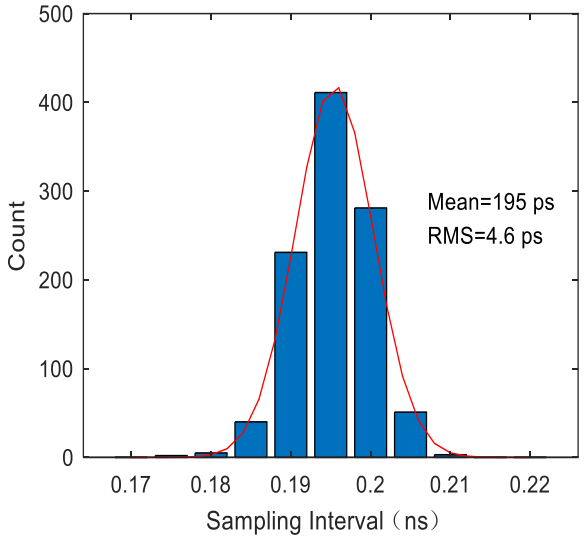


Sampling time interval

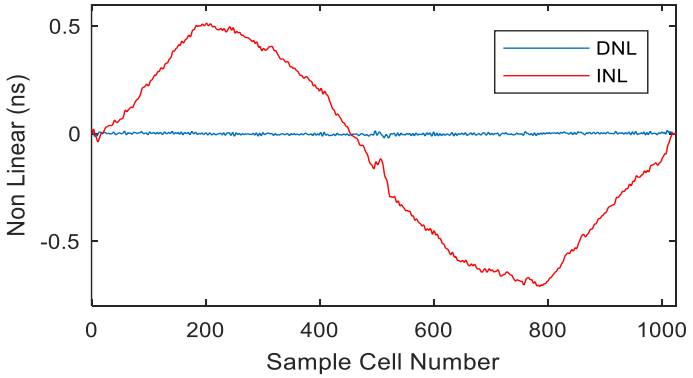
- Mismatch exists among sampling cells

  - Sampling interval
    - Mean: 195 ps
    - RMS: 4.6 ps

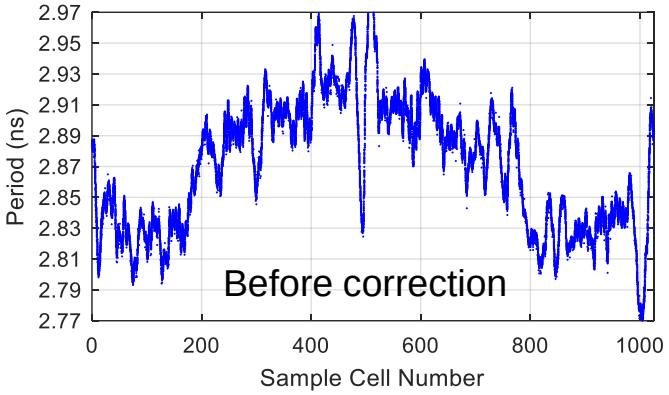


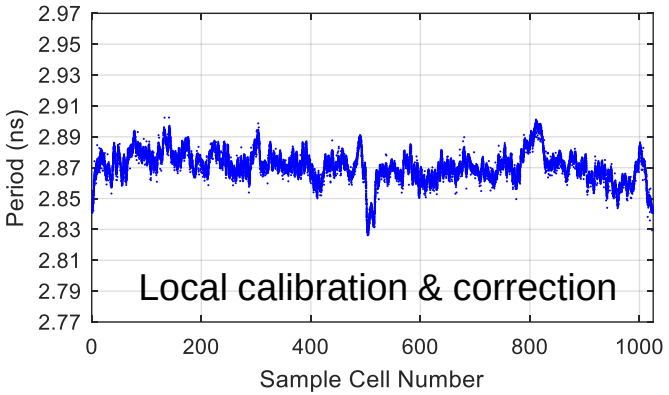


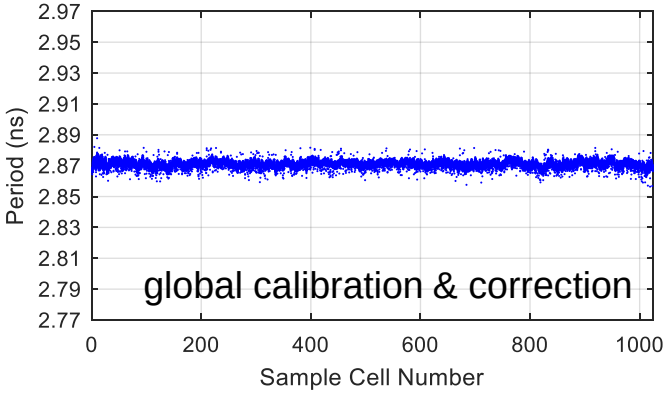
  - Non-Linearity:
    - INL: -709 ps ~ 513 ps
    - DNL: -19 ps~15.9 ps

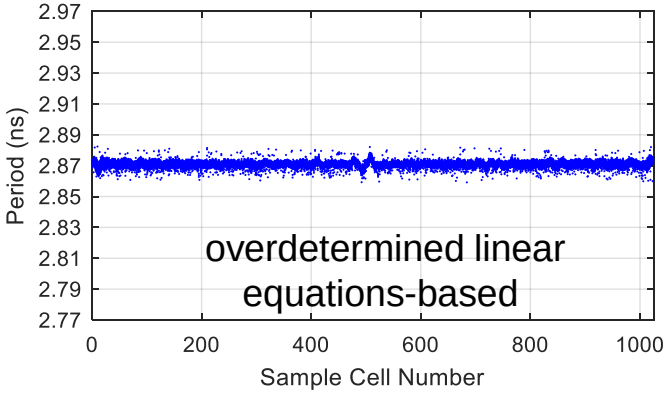


Time interval correction effect









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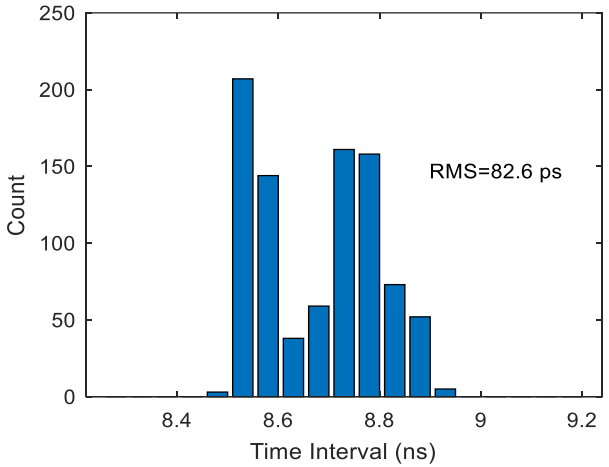
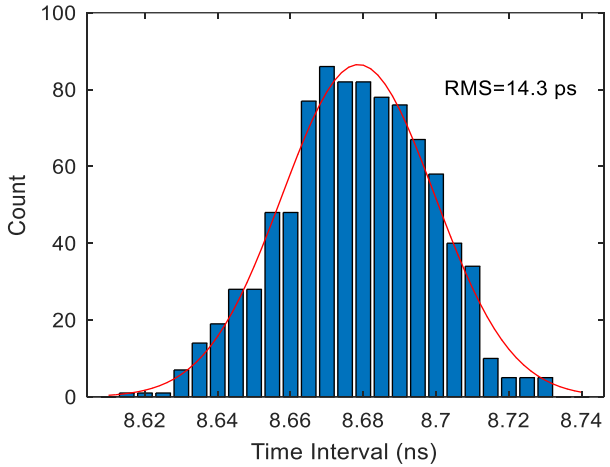
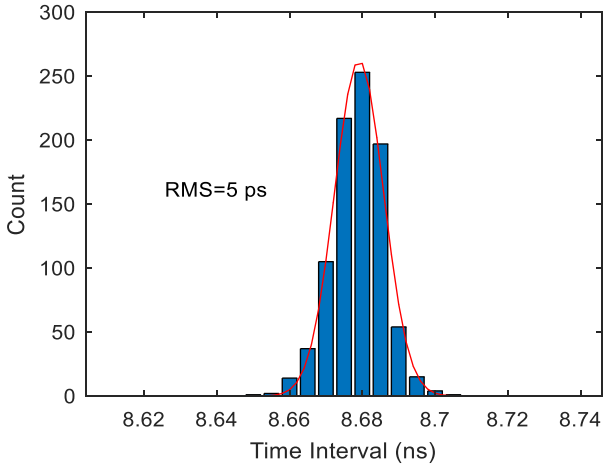
Time measurement performance



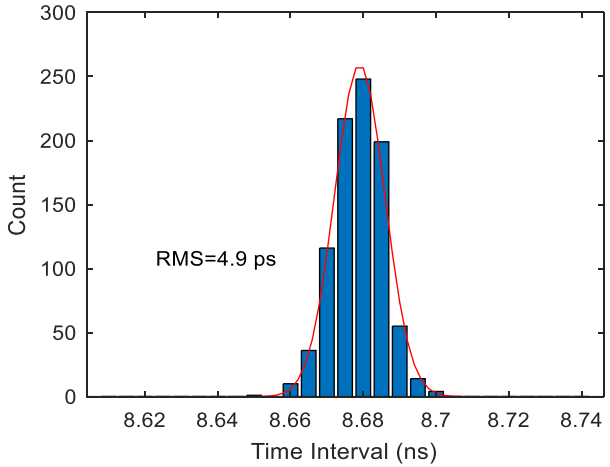
before correction, 82.6 ps RMS



Local calibration & correction, 14.3 ps RMS

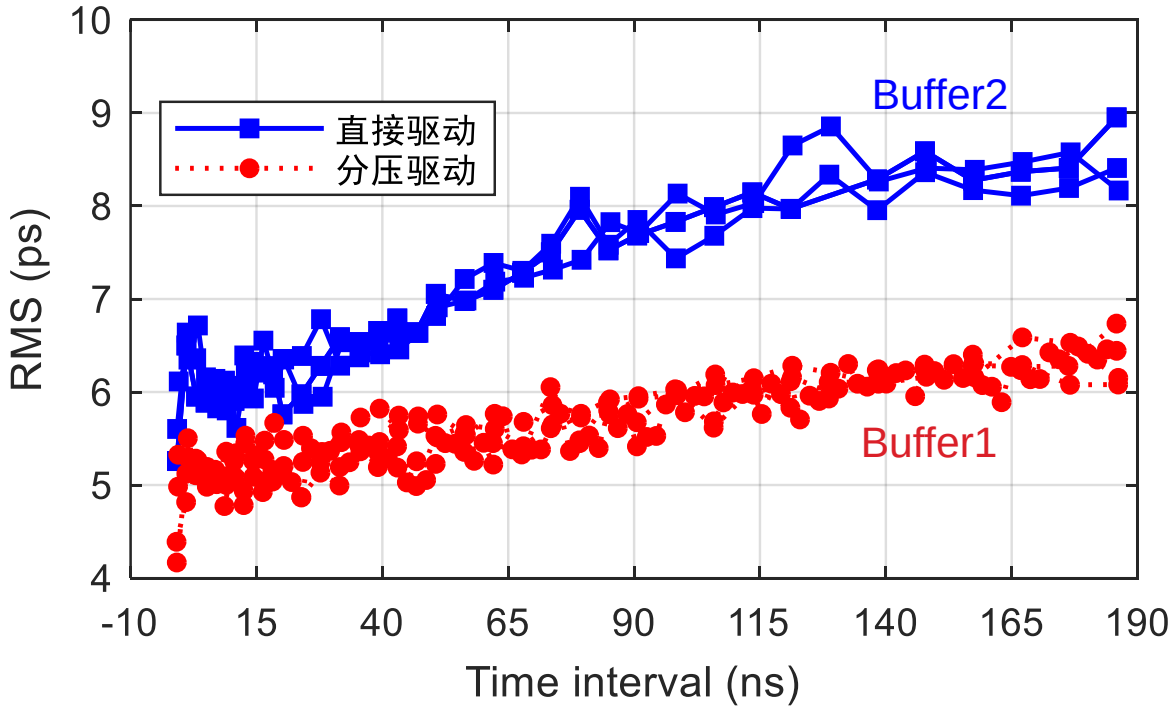


global calibration & correction, 5 ps RMS

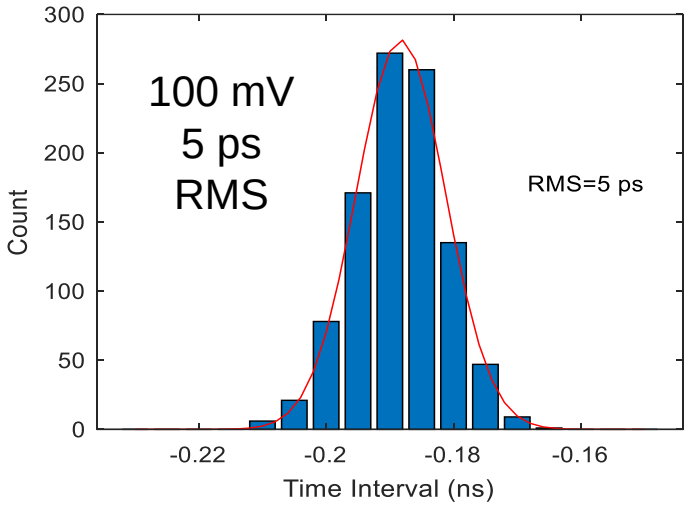


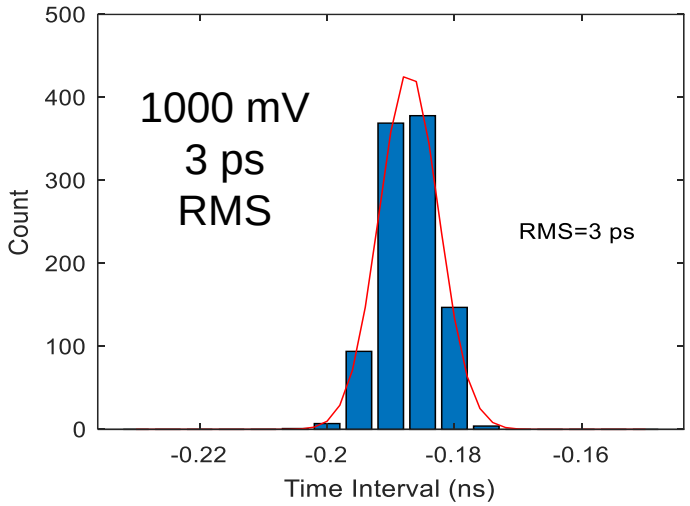
overdetermined linear equations-based, 4.9 ps RMS

Time measurement performance

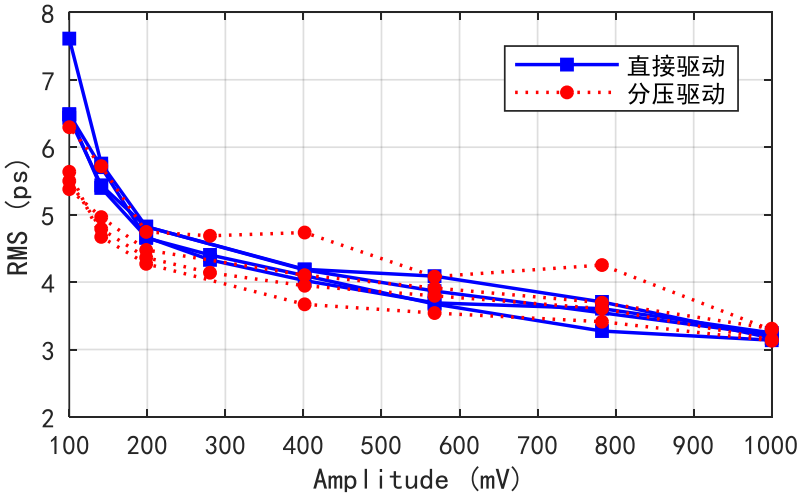


Time measurement performance



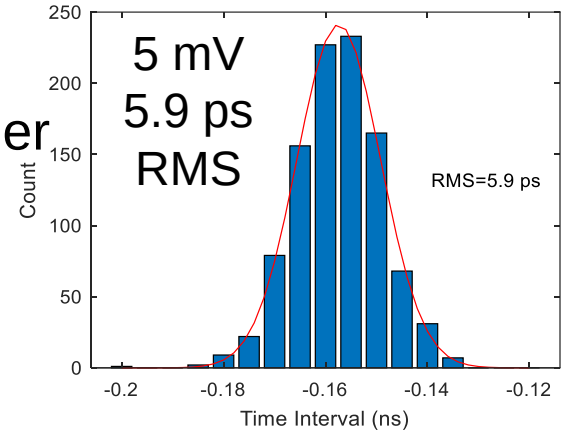


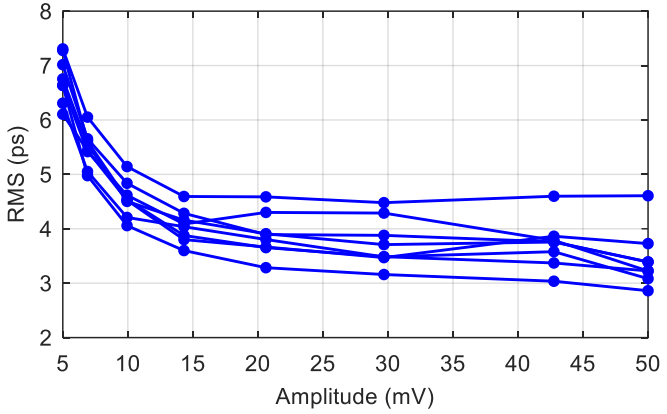
- Time resolution vs different input amplitude:
  - 100 mV：6.5 ps
  - 1000 mV：3 ps
  - 100~1000 mV：< 8 ps/ 7 ps



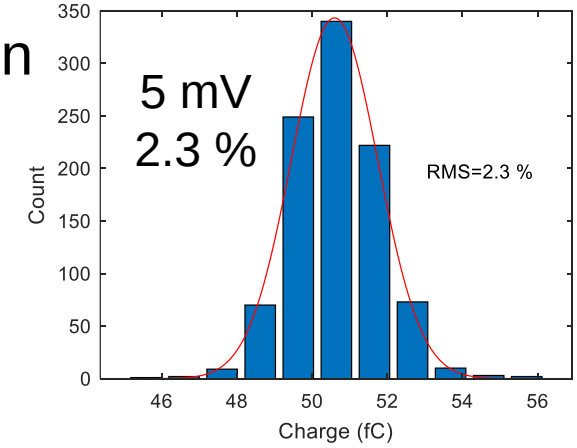
Performance test results

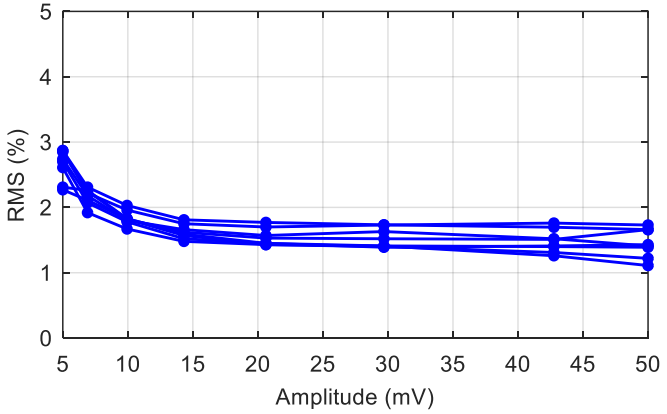
- Time resolution
  - Pre-amp+digitizer
  - <8 ps





- Charge resolution
  - <3 %





Conclusion

- Higher time precision is the key parameter of next generation MRPC and other fast detectors.
- Challenges for the readout electronics include high bandwidth, low noise, and high time precision.
- High speed waveform digitization is an important research direction, since all the detailed information can be obtained, and high precision time measurement can be achieved through digital signal processing on the digitized waveform.
- SCA-based waveform digitization exhibits low power consumption and complexity.
- Prototypes are designed and tested, and a time resolution of < 10 ps is achieved.
- Modification and improvement will be made on the electronics in the next version design.

Thanks!