GEM Readout R&D at USTC for SoLID Experiment

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Outline

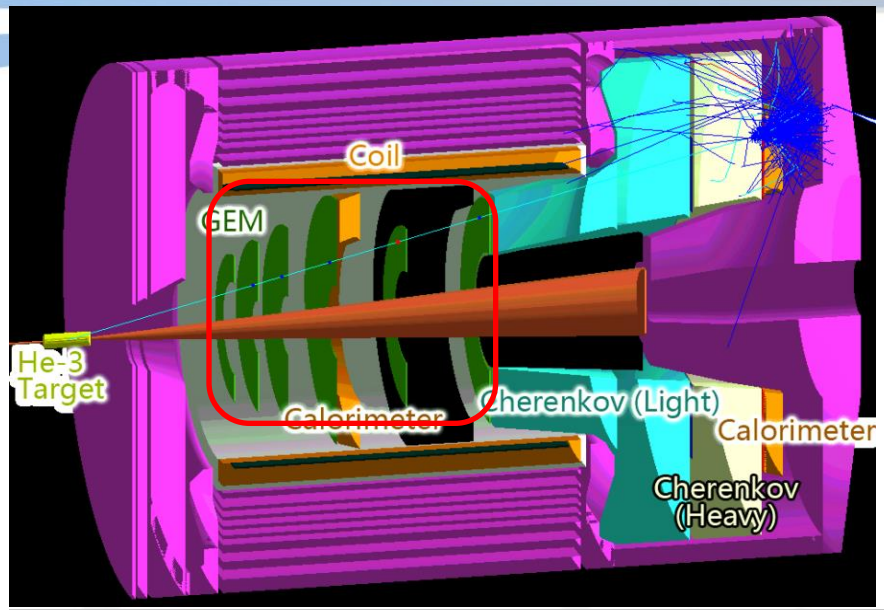
Background
- SoLID tracking system
- GEM readout requirement in SoLID

GEM readout
- GEM readout system on market
- GEM readout method used before
- new GEM readout R&D

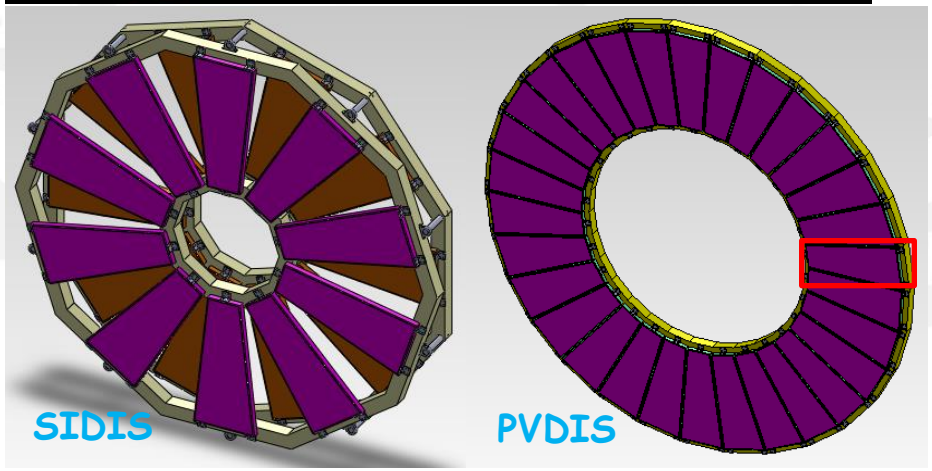
Our GEM readout
- GEM readout design
- FPGA logic design
- prototype board test
- new readout system plan

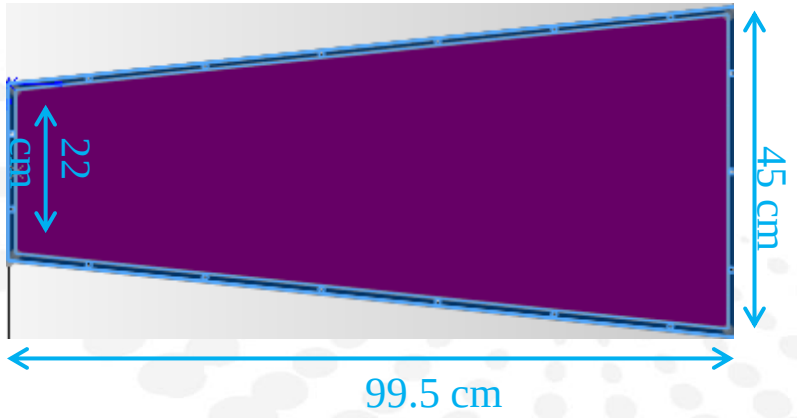
Conclusion and outlook

SoLID Tracking System



System Requirement	typical GEM
High Resolution: 100μm	~80μm
Large Area: 37m^2 in total	acheiveable
High Background Rate : 1MHz/cm^2	~MHz/mm^2





Large scale GEM

2 SoLID adopt GEM in the tracking system

Requirement to SoLID GEM Readout

PVDIS

Location	Z (cm)	R_{min} (cm)	R_{max} (cm)	Surface (m^2)	# chan
1	157.5	51	118	3.6	24 k
2	185.5	62	136	4.6	30 k
3	190	65	140	4.8	36 k
4	306	111	221	11.5	35 k
5	315	115	228	12.2	38 k
Total				$\approx$ 36.6	$\approx$ 164 k

SIDIS

Location	Z (cm)	R_{min} (cm)	R_{max} (cm)	Surface (m^2)	# chan
1	-175	36	87	2.0	24 k
2	-150	21	98	2.9	30 k
3	-119	25	112	3.7	33 k
4	-68	32	135	5.4	28 k
5	5	42	100	2.6	20 k
6	92	55	123	3.8	26 k
Total				$\approx$ 20.4	$\approx$ 161 k

large amount of readout channels: ~160k

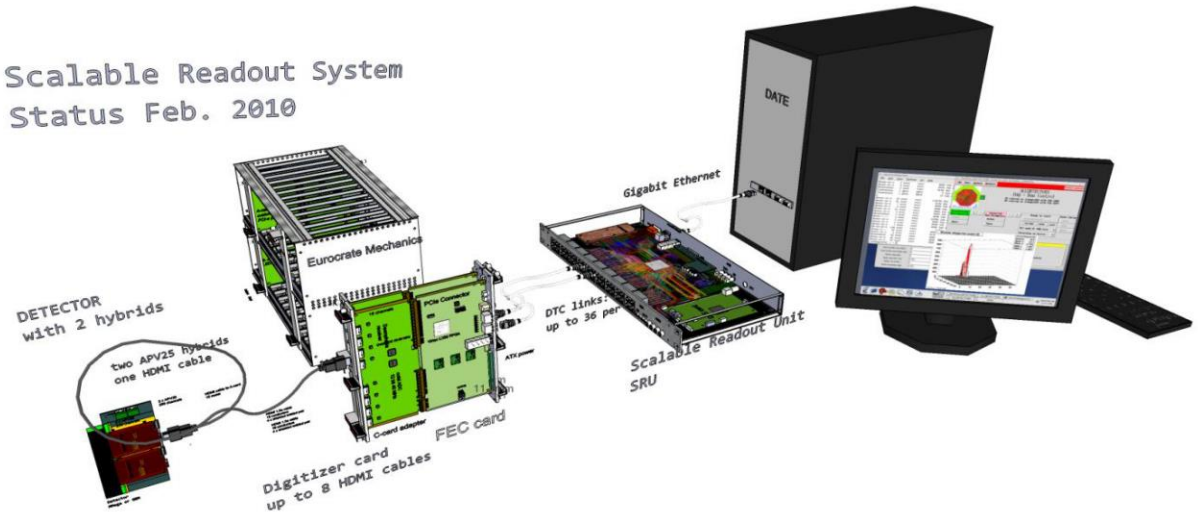
Table 1: Summary of Minimum Requirements of SolID Base Equipment

Equipment	dimension/description	description	performance, eff	performance, rej	conditions
Magnet	OD 3m, ID 1m, L> 3m	B> 1.35 T, BDL> 5 T-m	2π, 8 to 24° / 22 to 35°	P: 1-7 GeV, Res 2%	Fringe field < 5 G
GEMs	6 planes / 5 planes	Total 37 m^2, Chan 165K	Track Eff > 90%	Posi res 100μm	high rate
EM Calorimeter	1800 × 100 cm^2	18 RL + 2 RL +5 mm SPD	E res 10%, eff> 90%	50:1 π, 5:1 γ	rad hard
Light Cherenkov	2m CO2/ 1m C4F8O/N2	60 mirr, 270 PMTs, 20 m^2	γ-e > 10, Eff> 90%	π 500:1 < 4.5/3.2 GeV	100 G field
Heavy Cherenkov	1m 1.5 atm C4F8O	30 mirr, 480 PMTs, 20 m^2	γ-e > 10, Eff> 90%	K 10:1 2.5-7 GeV	100 G field
MRPC	50 × 3 modules, 10 m^2	1650 strips, 3300 chan.	Time res < 100 ps	K 20:1 < 2.5 GeV, γ 10:1	high rate
DAQ	282 FADC @ 250 MHz	32 pipeline VXS, 30 SRS	Trig 100 KHz × 2.6 KB	Trig 30 × 20 KHz × 48 KB	high noice
Lead Baffle	11 × 30 blocks,9 cm	5 cm, r 110-200 cm	area open ϕ > 4° / 12°	reduce background	

large amount of readout data

PVDIS	30 sectors	per sector trigger 20kHz	event size: 48KBytes
SIDIS	30 sectors together	trigger 100kHz	event size: 2.6KBytes

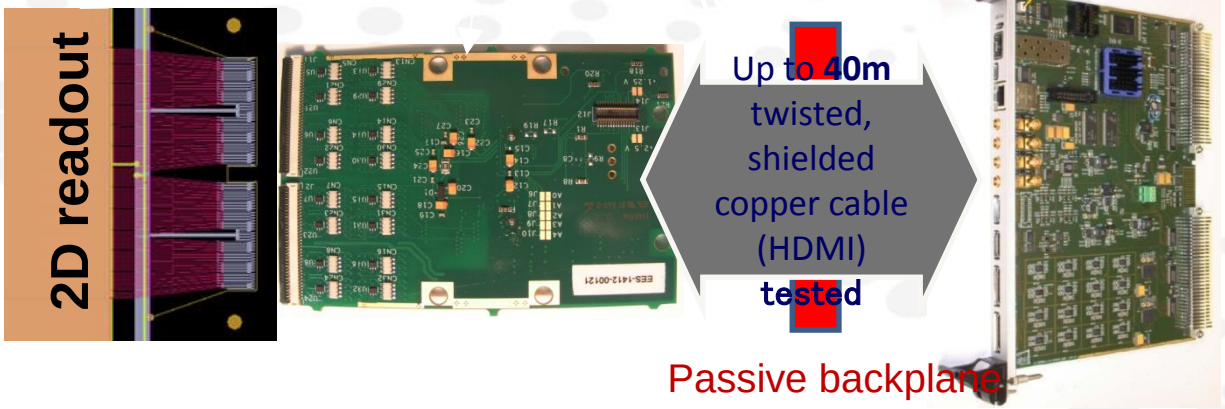
Readout System for GEM on Market



SRS

Both these systems are unavailable in USTC

GEM FEC 4.0 MPD



MPD

Both systems at work in UVa detector Lab

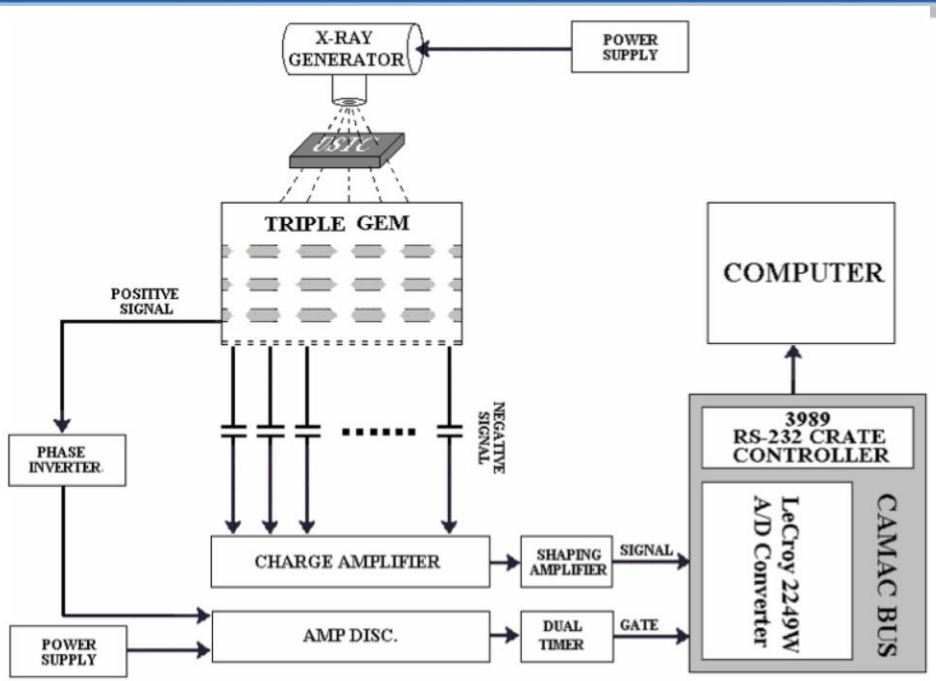
GEM Readout Method Used Before

❖Direct readout

σ_x~78μm

σ_y~86μm

X: 6 readout channels
Y: 6 readout channels

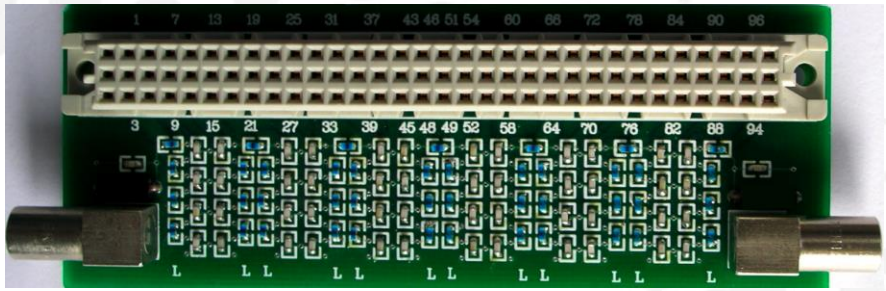


➢Readout few channels.
➢Cost too much.

❖Delay-Line readout

σ_x~148.4μm

σ_y~157.0μm



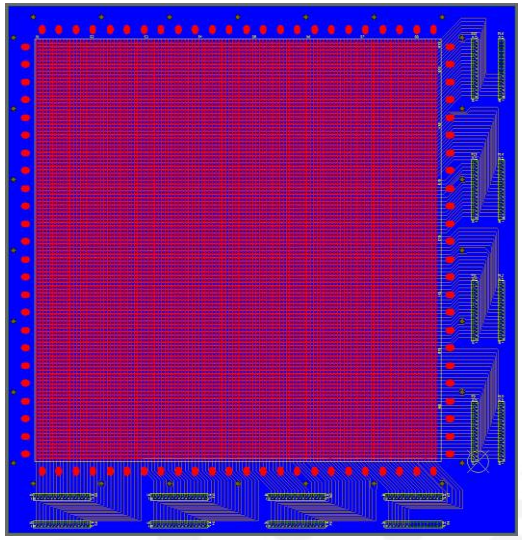
➢Low position resolution.
➢Low Speed.

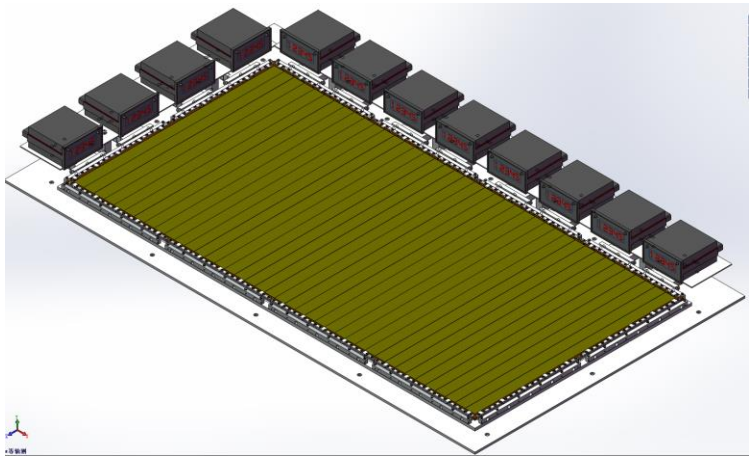
❖SFE16 based frontend readout

➢Suitable for small GEM readout.

We Need New GEM Readout System

USTC GEM R&D in great progress





30cm*30cm GEM detector

future design: 1m*0.5m GEM

Two-dimension readout:
118 readout strips in x direction;
118 readout strips in y direction.

Why new readout?

- MPD system we bought still has some problems.
- GEM readout method we used before could not satisfy the requirement to large GEM R&D

Our Readout System:

- easier to use, for testing GEM prototype
- R&D MPGD readout system

GEM Readout System Design

APV_MRS(Multiple_chip Readout System):

- APV MPD structure
- INFN APV FrontEnd
- USB, PCI connector, easier to test and debug
- new FPGA code

Character:

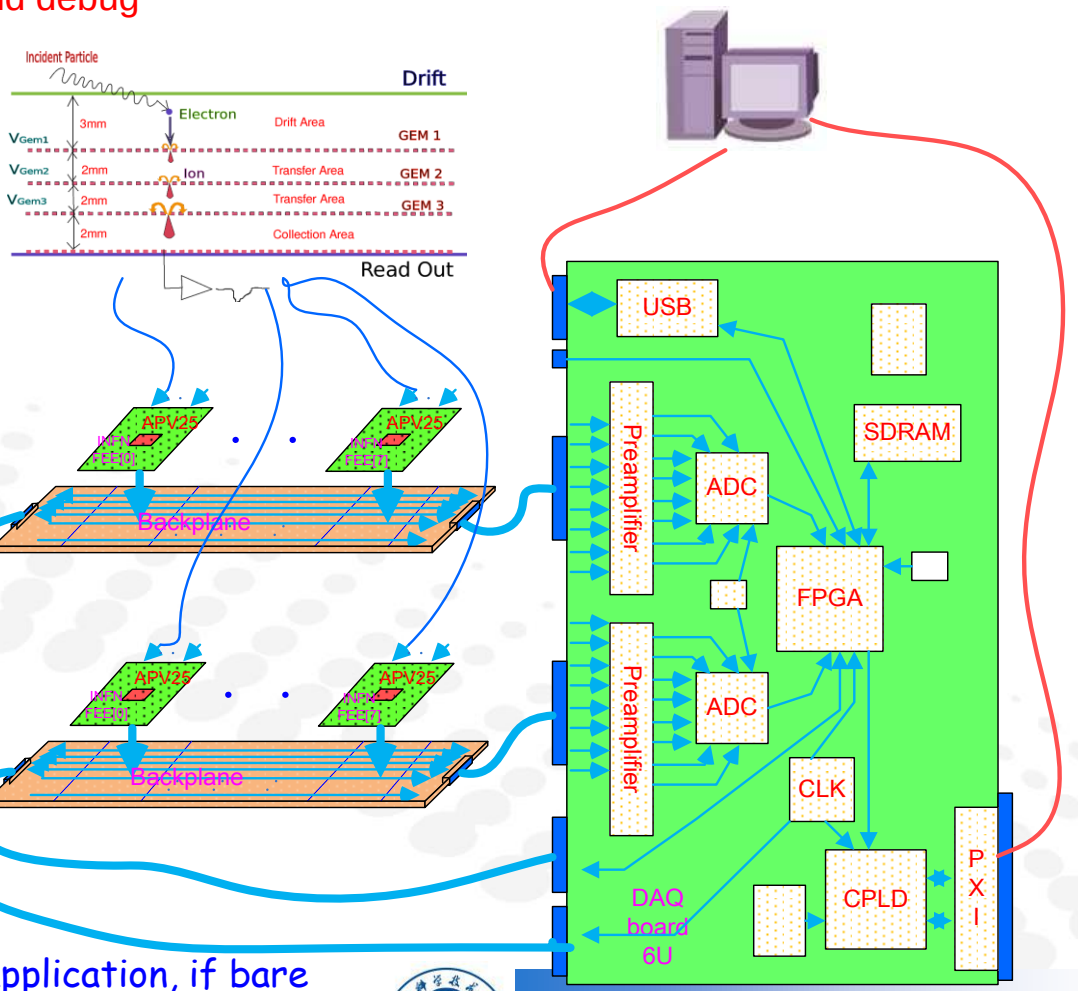
- Digitalization of 16 APVs, 2048 GEM channels.
- Maxium APV acceptable trigger rate is 270kHz.
- Maxium data rate for PCI is 132MBps, for USB is 60MBps

satisfy SoLID requirement

Demand:

- SoLID only needs 80 MRS boards in total.
- USTC GEM test needs one MRS board.

APV_MRS
(Multiple_chip Readout System)



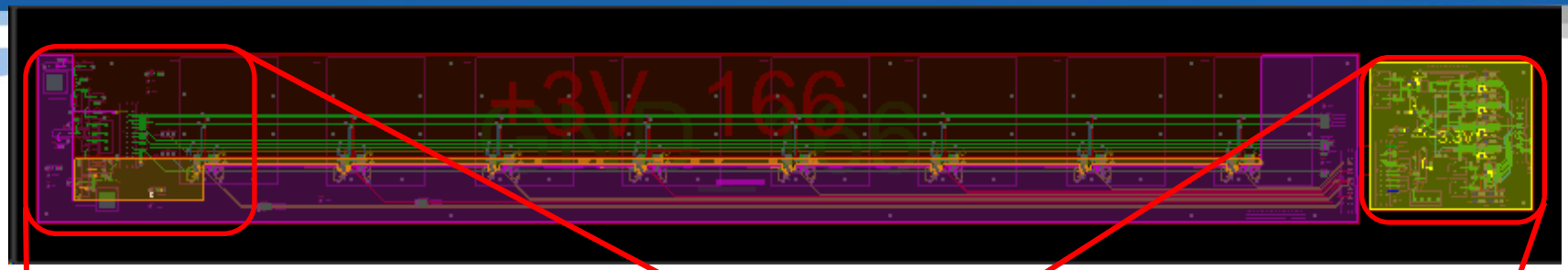
APV chip liscense is in application, if bare chip is available, we hope to build new APV FEE.

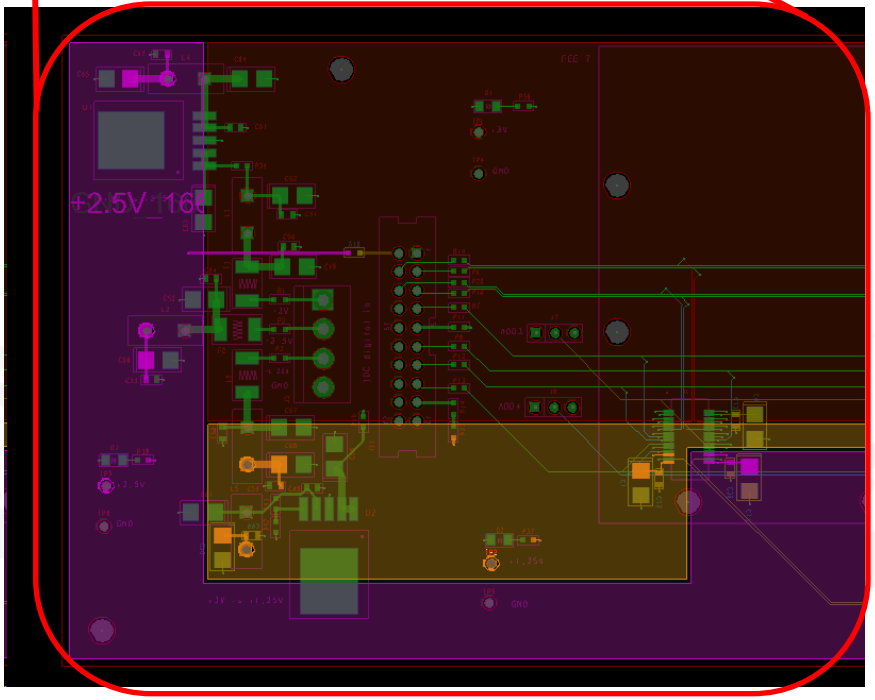
MRS Prototype

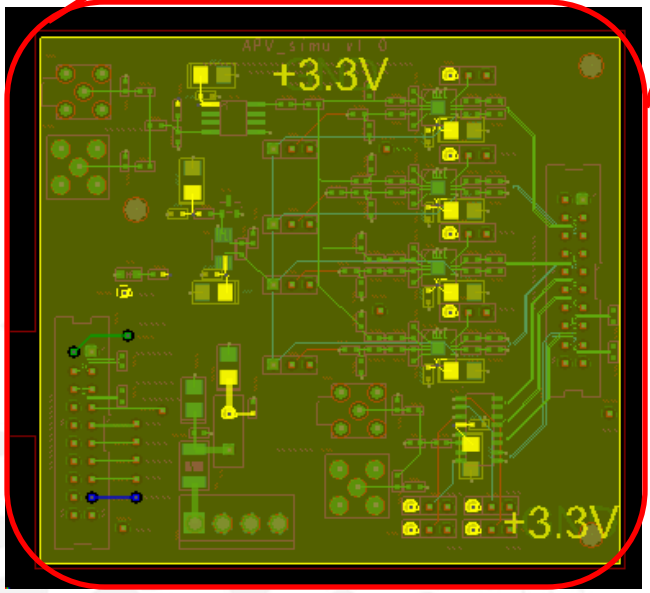
Top View

Bottom View

APV backplane







APV backplane
- 8 APV FEE slots
- test points and power supply

APV simu board
- simulate APV FEE output signal
- test MRS performance

APV backplane board:
- PCB design is finished and is in manufacture now.

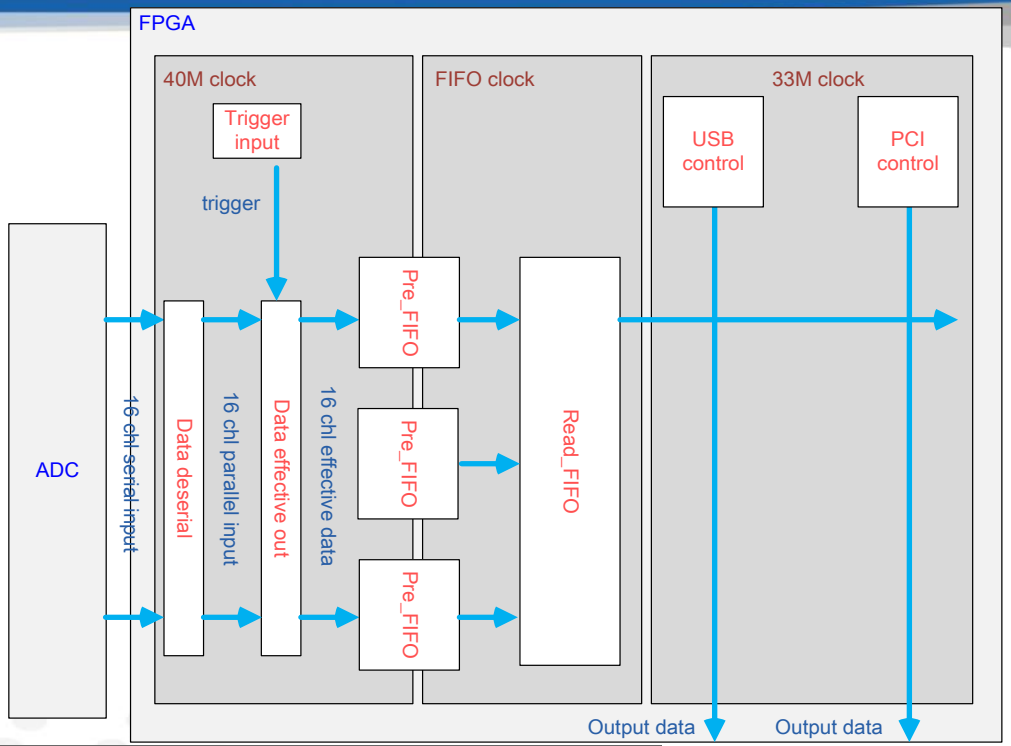
MRS FPGA Logic Design

Logic Design:

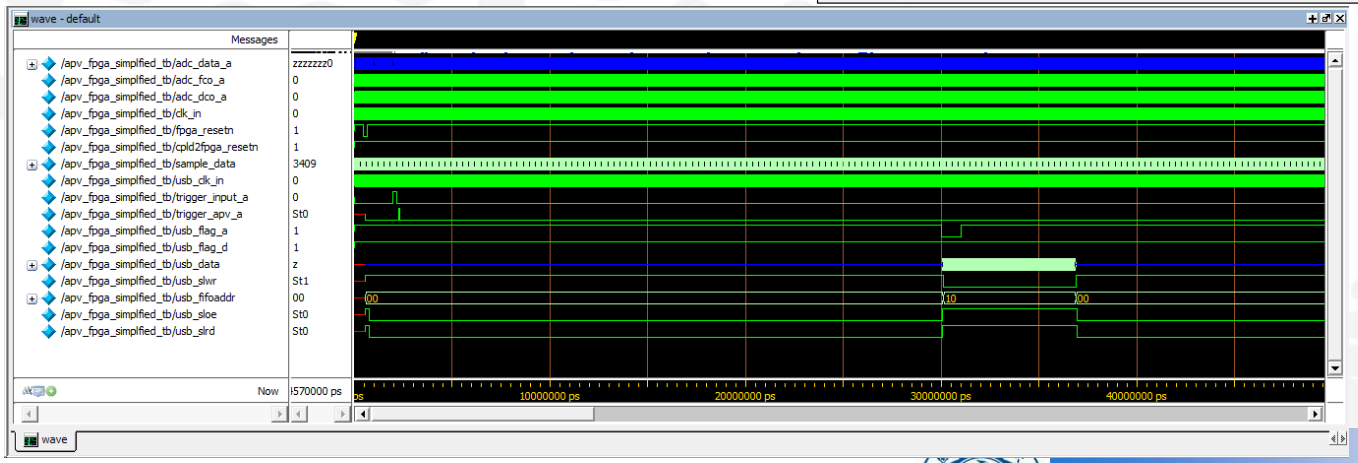
- FPGA logic schematic is finished
- Simplified FPGA logic version coding is done
- Simulation is done, code works well

APV_FPGA_simplfied:

- Flexible channel output control
- APV control
- APV raw data output



simplified FPGA logic schematic



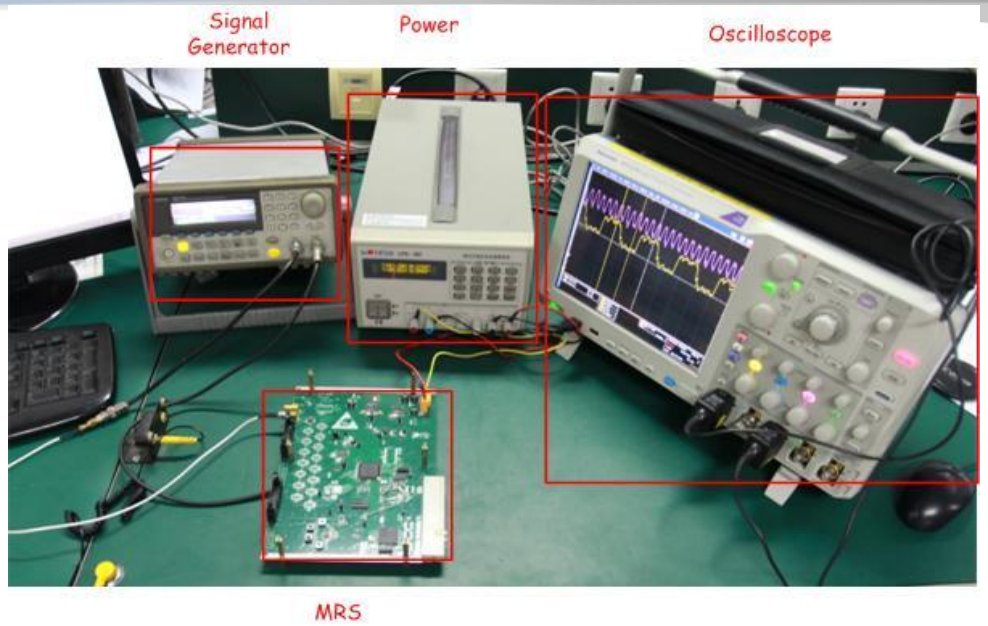
FPGA logic Modelsim simulation

Test result and further work

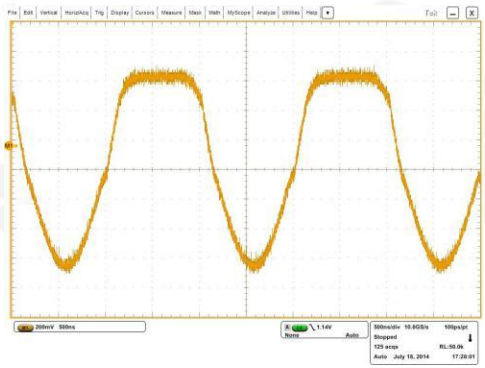
Current result:

- Clock, ADC, FPGA works well
- FPGA logic is implemented
- Preliminary data sampled by Signal Tap II

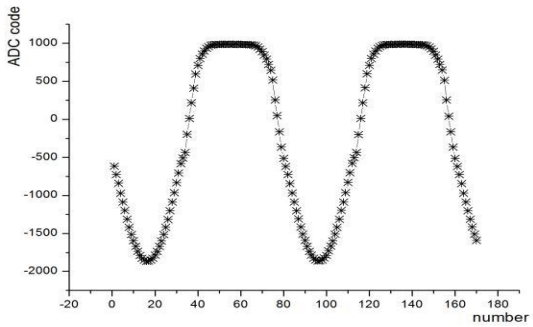
- USB port and PCI is under test



MRS test platform



waveform from oscilloscope



data from FPGA

Further work:

- backplane to be manufactured
- MRS analog performance to be tested

- PCI data transport test, MRS performance test
- FPGA logic to be finished and ungraded

MRS FPGA Logic Ungrade Plan

Reason to Logic ungrade:

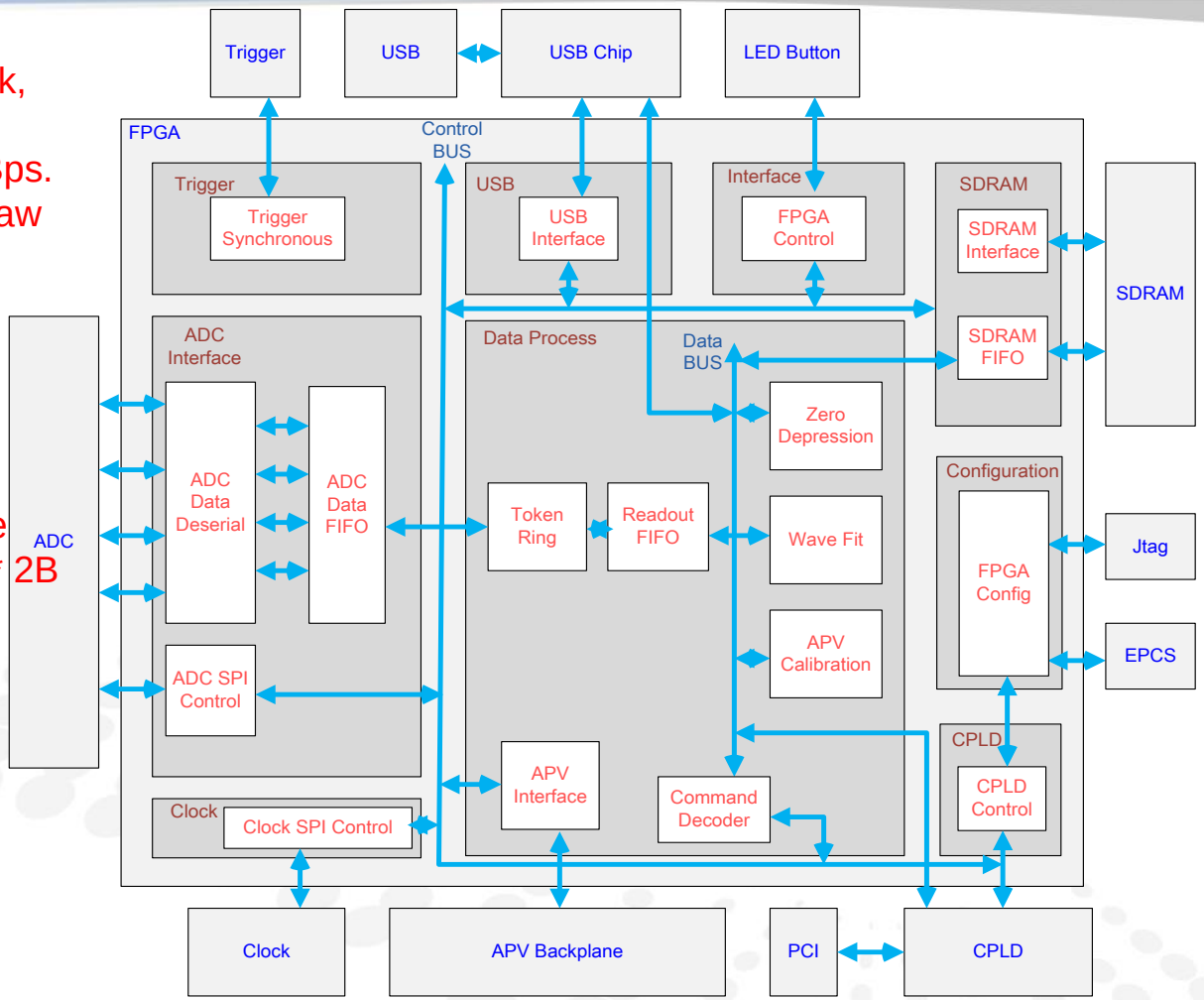
- one trigger 2 bytes, trigger rate 100k, raw data rate = 100k * 16chips * 3samples * 128chls * 2B = 1228.8MBps.
- it is impossible to transfer 16 APV raw data constantly.
- A lot of useless data is transferred.

It is necessary to use on board data compression.

- one trigger read out 5 chls, effective data rate is 100k * 5chls * 3samples * 2B = 3MBps
- this data rate is acceptable

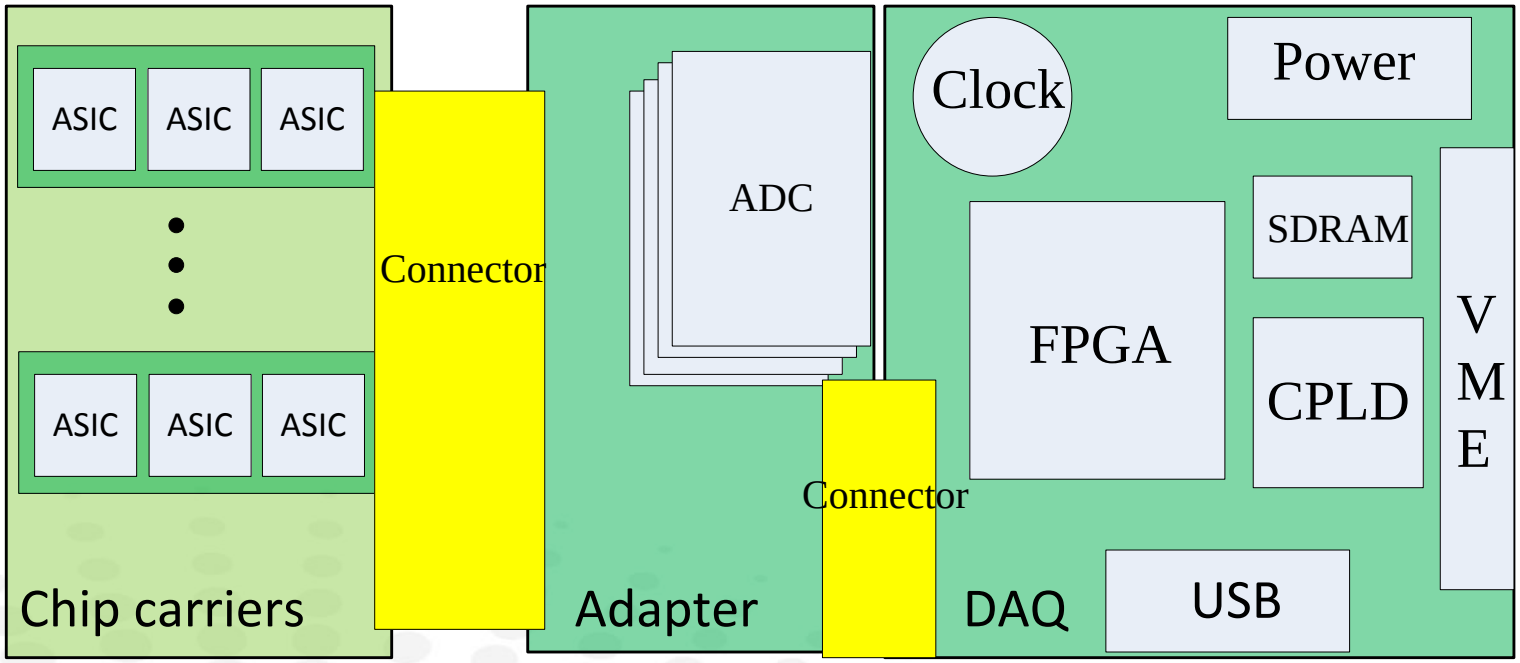
Logic Ungrade:

- Common Mode Substraction
- Baseline Correction
- Data zero depression



MRS FPGA logic diagram

New Readout System Plan



New Readout System diagram

New System:

- SRS architecture
- Three boards: Chip carrier, Adapter, DAQ
- Use different ASIC chip we can get
- simplify readout design, use in different experiment situations

Conclusion and Outlook

Conclusion:

- New GEM readout system R&D is required.
- The APV MRS design is finished, prototype board is manufactured.
- The APV backplane and test board design is finished.
- The simplified version of logic is finished, and its simulation is done.
- APV MRS board is under test, no function problem.

What to do:

- Further testing of MRS function and performance.
- New logic design and its simulation.
- Test of backplane and FEE in the near future.
- Detector and electronic system test.

- New readout system R&D in the future.

Thank you!