DAQ & Electronics for the CW Beam at Jefferson Lab

Benjamin Raydo

EIC Detector Workshop @ Jefferson Lab

June 4-5, 2010

Goals for EIC Trigger

High Event and Data Rates

- Trigger must be able to handle high luminosities (and hadron multiplicities)

- Trigger rate depends on e-p interaction rate ($\mathcal{L}\sigma$), not bunch crossing frequency
  - events will be read out when trigger occurs
  - as in CLAS, the time reference is provided by tracking the electron (stable β=1 particle)

Other Requirements

- High efficiency for rare triggers and low electron energies
- Minimum-bias trigger with limited (if any) prescale for low-Q^2 events
- Random background suppression at levels 1 & 2 (track vertex reconstruction, etc)

Rate estimates

- H1/ZEUS at 5 x 10^{31}: < 1000 Hz @ level-1, 10 Hz @ level-3 to tape
- CLAS12 at 10^{35}: 10 kHz @ level-1 to tape (mostly π- due to low Cerenkov thresholds)
- EIC at a ~10^{34} (estimated): 100 kHz @ level-1, 10 kHz to tape

Implementation can be based on JLab 12 GeV trigger experience

- High-rate capability (200 kHz) from GlueX hadron trigger
- Advanced algorithms from CLAS12 trigger

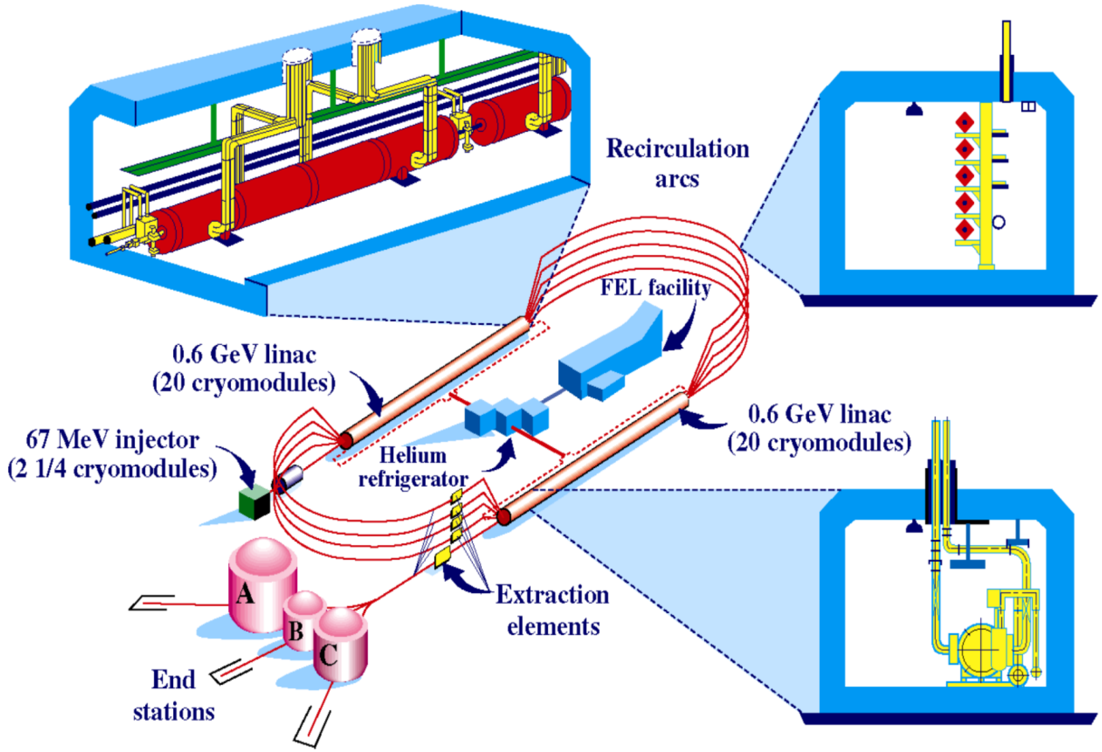
CW Trigger Talk Overview

1. JLab CW Accelerator Facility
2. Pipelined Trigger Overview
3. Pipelined front-ends: Flash ADC
4. Forming Triggers
5. Trigger Implementations at JLab

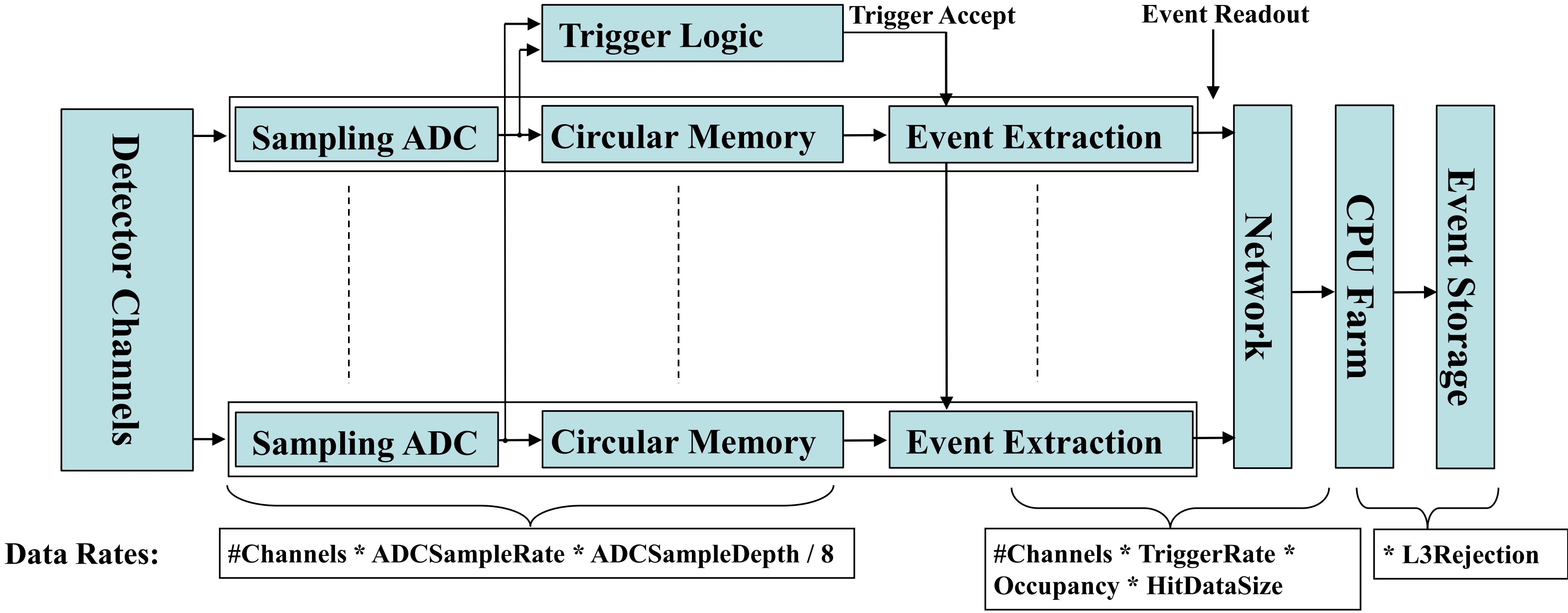
1.0 JLab CW Accelerator Background

CEBAF

- Two recirculating Linacs operating at 1497MHz
- Three beams produced at the injector with 120 degrees of phase separation
- Beams delivered to three experimental halls at 499MHz
- Continuous Wave (CW) bunches at ~2ns on fixed targets



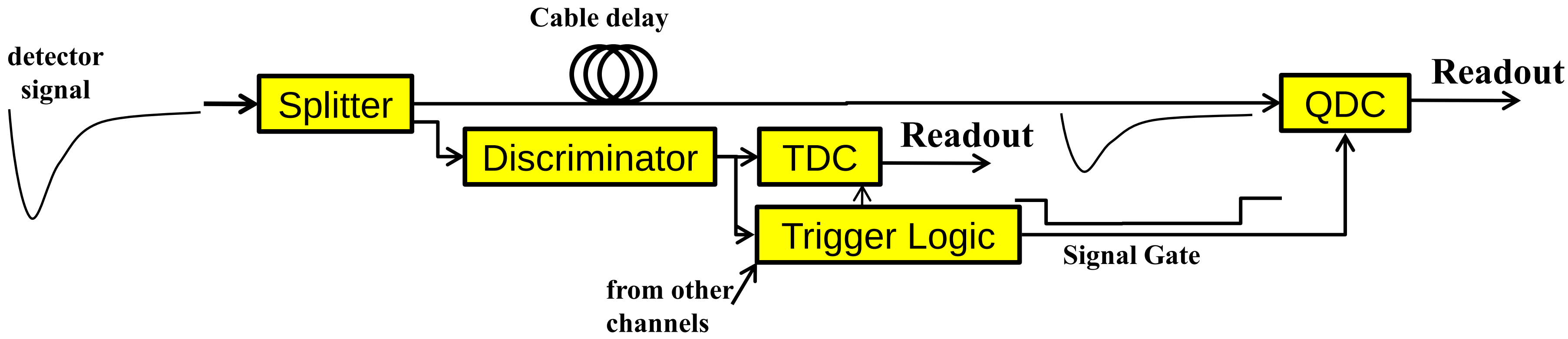
2.0 Pipelined DAQ & Trigger Architecture



- All channels are continuously sampled and stored in a short term circular memory

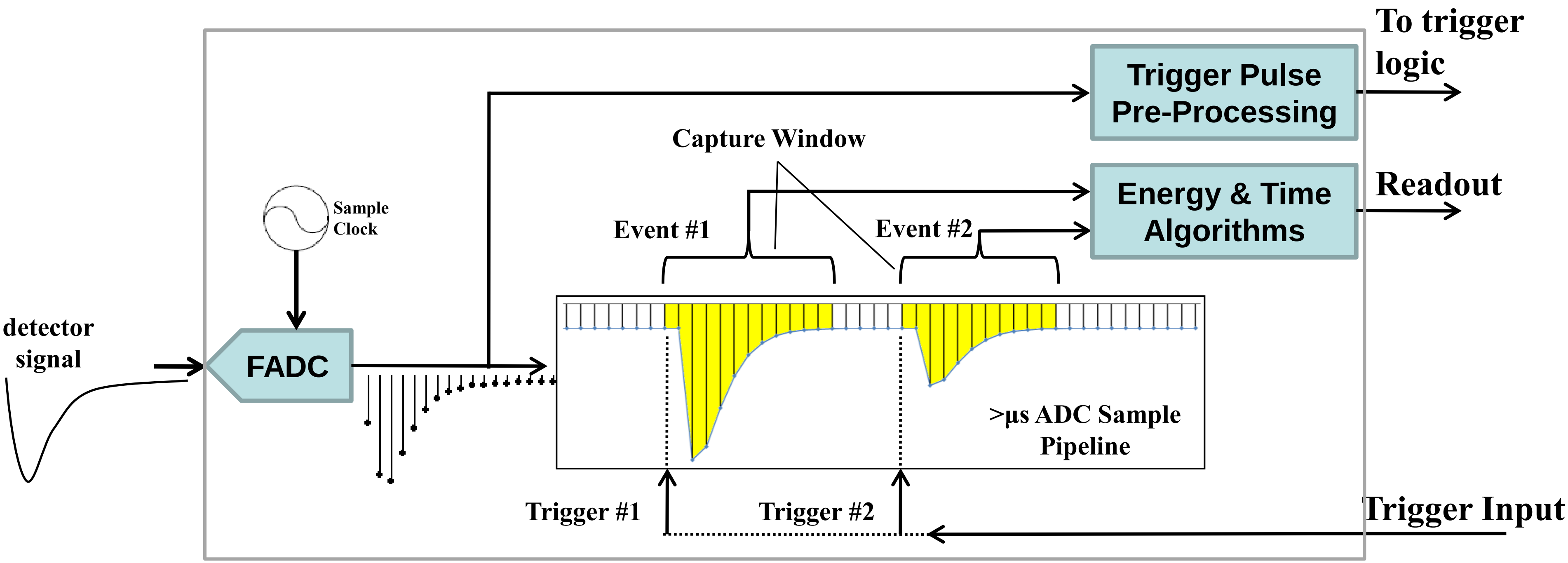
- Channels participating in trigger send samples to trigger logic. When trigger condition is satisfied, a small region of memory is copied from the circular memory and processed to extract critical pulse details such as timing & energy. **This essentially makes the event size independent of ADC sampling rate, depth, and number of processed points.**

3.0 Traditional Method of Signal Capture



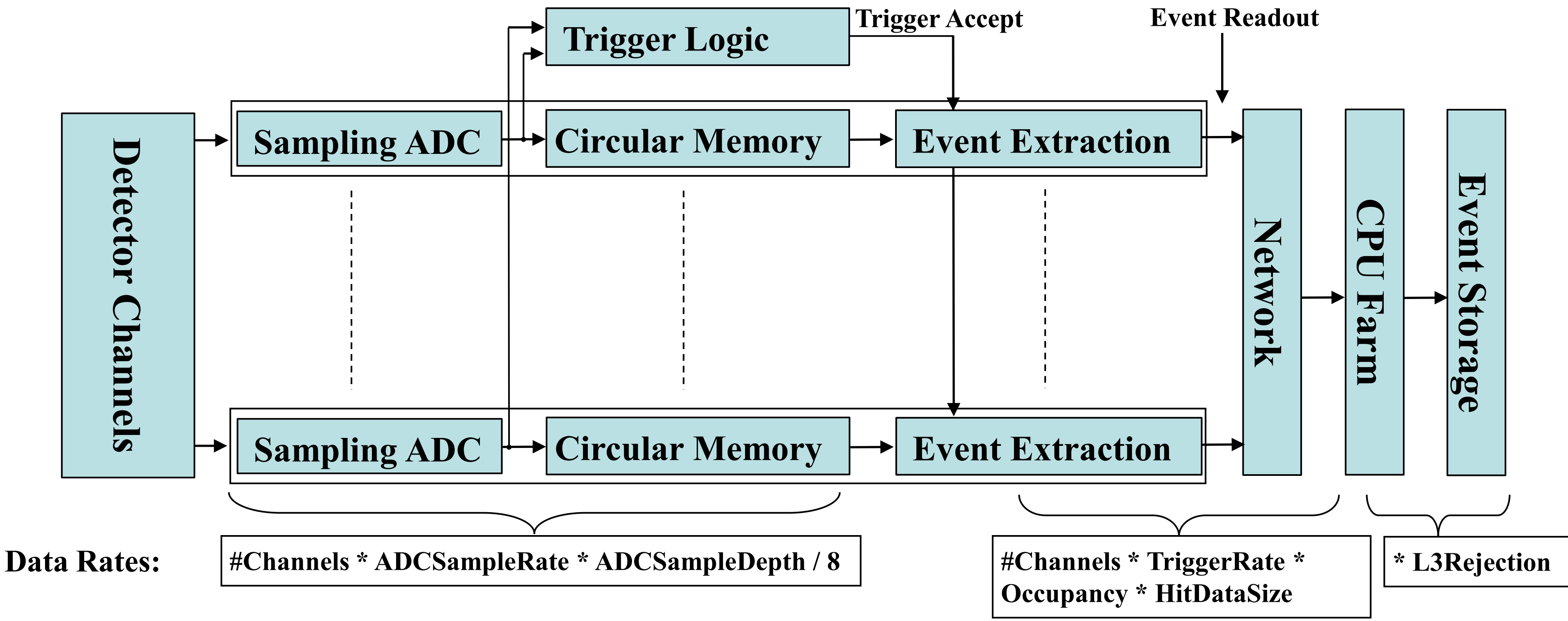
- Requires multiple modules to acquire time and/or charge
- Detector signals must be delayed to allow trigger decision time to form gate
- Very limited trigger logic resolution or very complex/expensive to build
- Gated readout modules typically have large conversion times, creating dead-time

3.1 Modern Method of Signal Capture



- Sampling Flash ADC stores digitized signal in large memory with trigger decision made
- Trigger input copies a window of the pipeline and extract pulse charge and time for readout
- Trigger output path contains detailed information useful for cluster finding, energy sum, etc.
- **Hardware algorithms provide a huge data reduction by fitting and reporting only time & energy estimates for readout instead of raw samples**

3.2 Pipelined DAQ & Trigger Architecture



For example, the Hall D GlueX Experiment we can calculate the following:

125Msps 12bit ADC: ~13,000 channels => 13,000 * 125,000,000 * 12 / 8 = 2.4375 TB/sec

250Msps 12bit ADC: ~6,000 channels => 6,000 * 250,000,000 * 12 / 8 = 2.25 TB/sec

A total of ~5 TB/sec directly from detector. However:

Expected trigger rate is <200kHz, Occupancy ~6%, HitChannelEventSize ~18bytes, L3Rejection ~10

Readout total of ~3GBytes/sec. Farm rejection factor 10 => ~300MBytes/sec to disk.

3.3 JLab Pipelined Flash ADC

- 16 Channel 12bit, 250Msps Flash ADC
- 8µs raw sample pipeline, >300kHz sustained trigger rate (bursts @ ~15MHz)
- Post-processing in customizable firmware to extract time, charge, and other parameters minimizing event size
- Module supports 2eSST VME transfers at 200MB/s transfer rate
- Large event block sizes (>100) to minimize CPU interrupt handling
- VXS P0/J0 outputs 5Gbps L1 data stream (hit patterns & board sum)

- Used in existing 6GeV program:

    Hall A BigBite & Moller Polarimeter

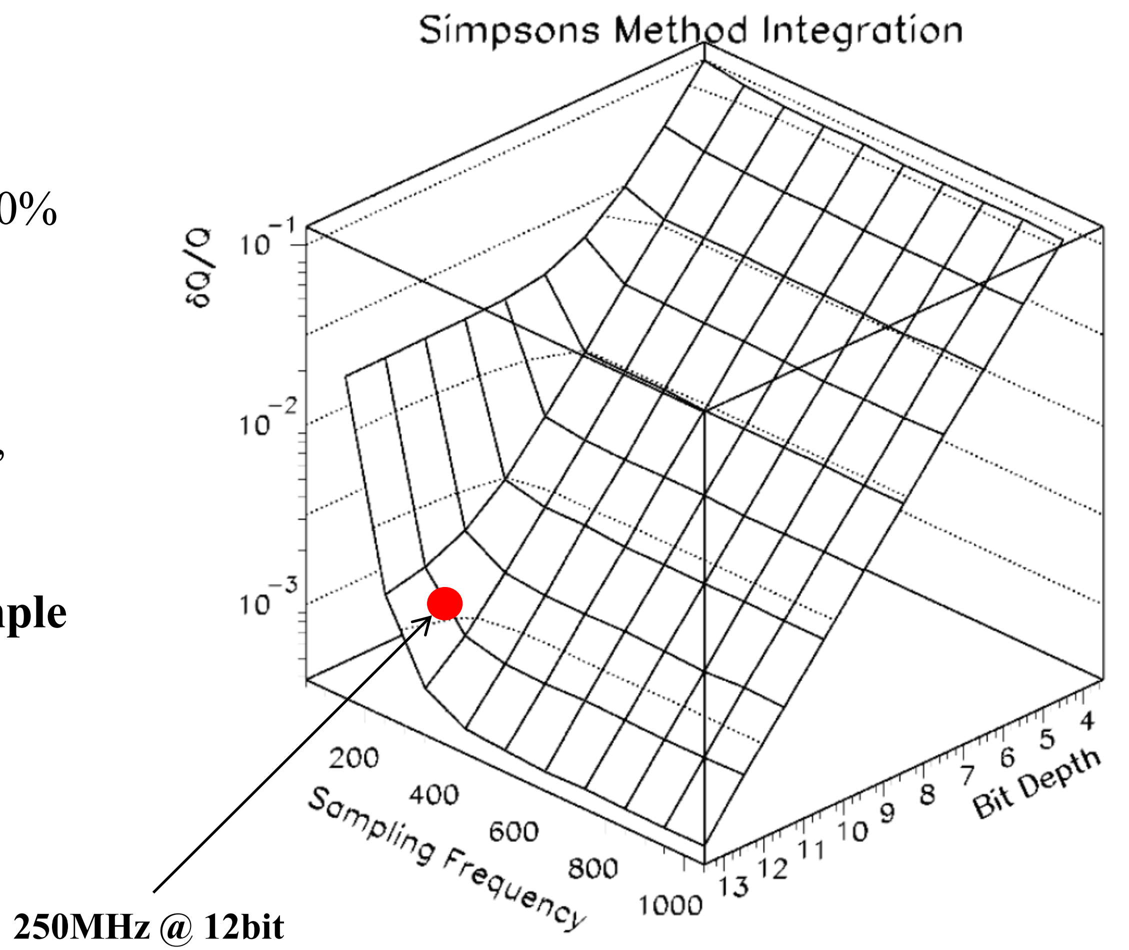
3.4 FADC Sampling – Charge Accuracy

Hall D FCAL PMT: FEU 84-3

-10,000 Random height pulses 10-90% full scale of ADC range simulated

- Sampling frequency makes little difference beyond 250MHz at 12bit, providing ~0.1% charge resolution

- PMT pulse shape dominates sample frequency and bit depth of ADC



From: GlueX Doc# 425-v1

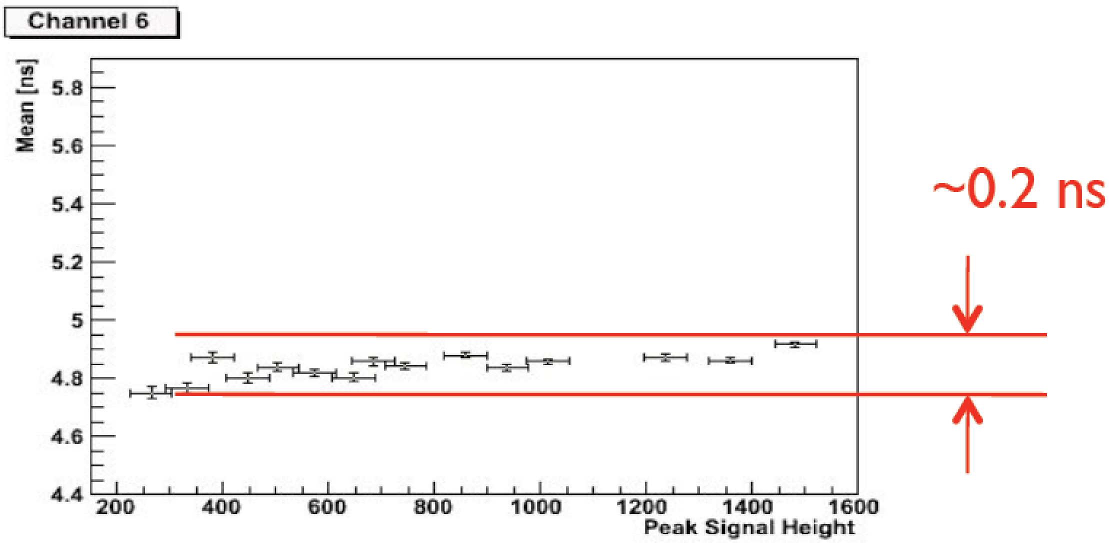
3.5 FADC Sampling – Timing Accuracy

Hall D FCAL PMT: FEU 84-3

- Timing algorithm developed & tested by Indiana University for the Hall D forward calorimeter.

- Implemented on the JLab FADC250 hardware achieving <300ps timing resolution on 50% pulse crossing time with varied signal heights.

- Resolution allow reliable information to link calorimeter with tagged electron bunch.



Typical timing resolution achieved ~1/10 the sample rate. The PMT shape will drive the ADC sample rate & depth requirements.

From: GlueX Doc# 1258-v1

4.0 Forming Triggers

Rate = $\mathcal{L}$ x σ_T ~ 100kHz for EIC@JLab

- Bunch crossing rate of 1.5GHz and Interaction rate of ~100khz we get an **e-p interaction of interest every ~10^4 bunch crossings**

- A trigger occurs when trigger condition is satisfied, which is computed asynchronously with bunch crossing.

- As in CLAS, the time reference is provided by tracking the electron (stable β=1 particle)

Hardware Triggering Options

Background suppression achieved by using advanced triggers:

- Calorimeter cluster finding (sliding window, cluster size & energy)
- Track reconstruction (Shift/sum methods, Hough transform, vertex finding)
- Geometrical matching between detectors

JLab is experienced in these types of trigger designs (6GeV and 12GeV trigger designs)

5.0 JLab Trigger Designs

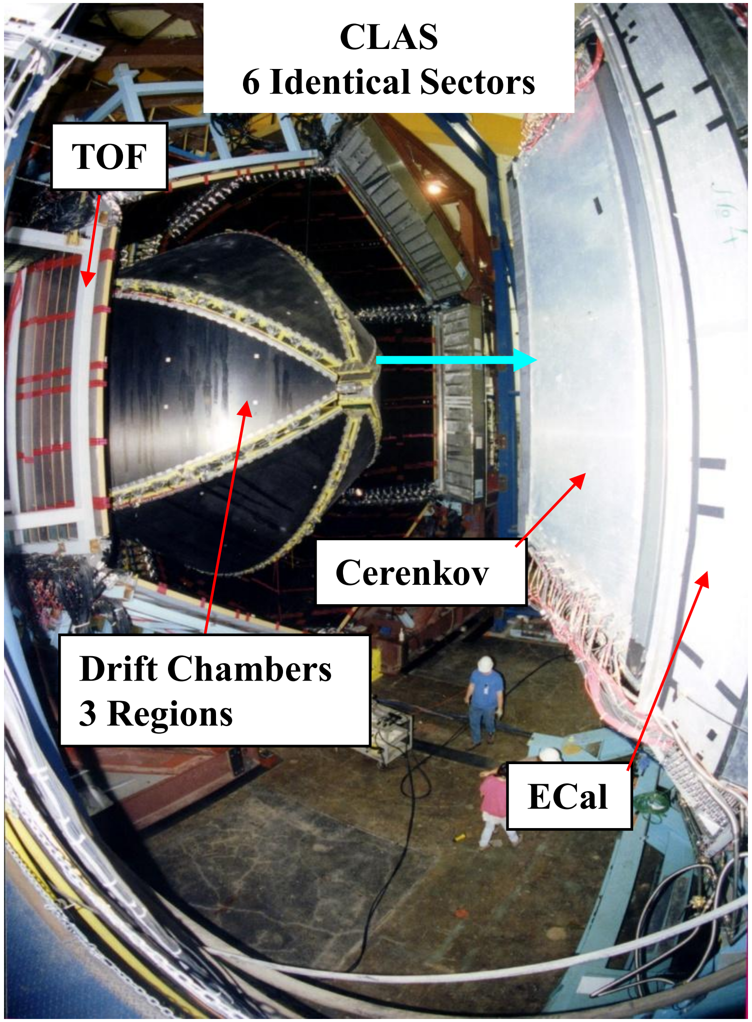
Existing CLAS Trigger

12GeV Pipelined Trigger Designs

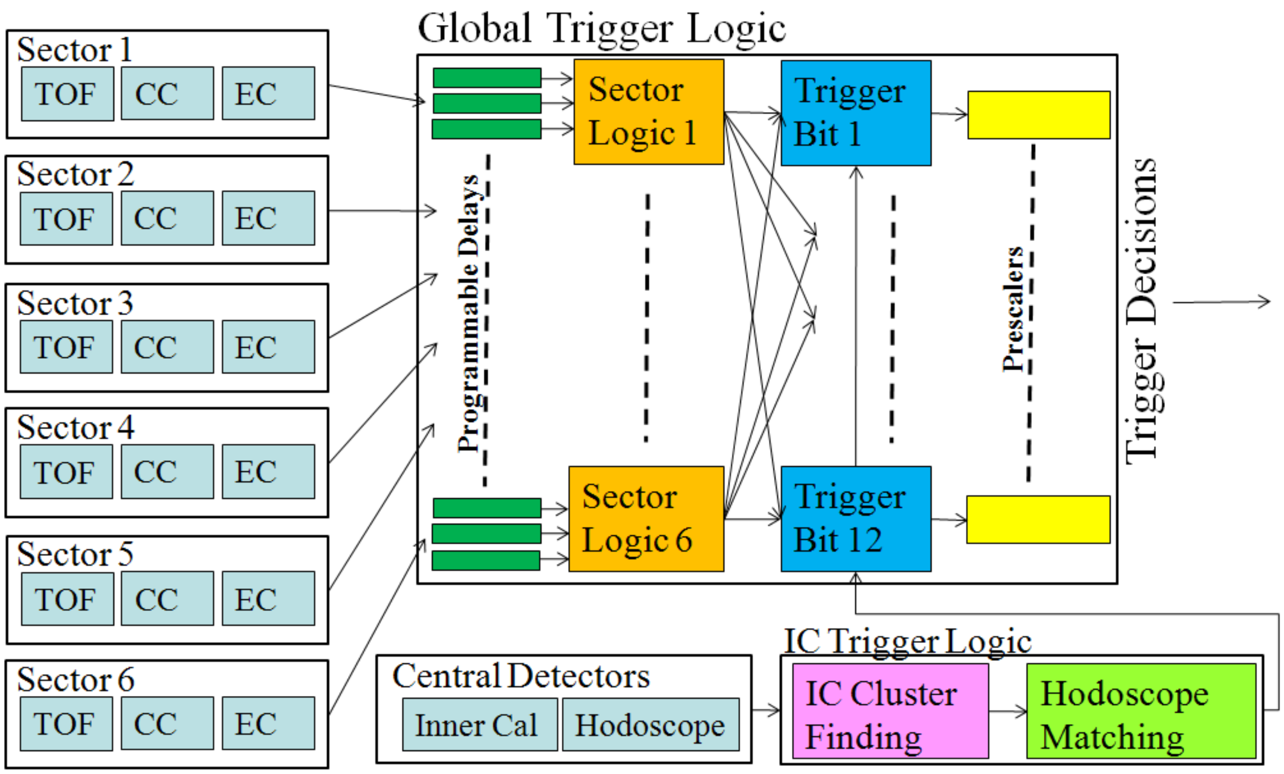
5.1 CLAS Detector & Trigger

- Photon & Electron Experiments with polarized targets, polarized beam
- High Luminosities a few x$10^{34}cm^{-2}s^{-1}$:
- DAQ event rate designed to ~10KHz
- FPGA based Level 1 Hardware
  - Pipelined design (5ns pipeline clock)
  - Low latency (~150ns)
- Fast Level 1 for ADC Gate, TDC Start
  - TOF, Cerenkov, Electromagnetic Calorimeter
  - Pattern recognition programming
  - Sector based logic for L1 trigger 'equations'
  - Cluster finding for Inner Calorimeter

•Up to 32 Front End ROCs
  - Fastbus, VME, [TDC; ADC; Scalers]



5.2 Existing CLAS Trigger



- Fast L1 trigger design for CLAS
- Sector based triggers combined with central detector information
- Very fast cluster finding trigger for Inner Calorimeter (IC)

5.3 IC Cluster Finding Trigger

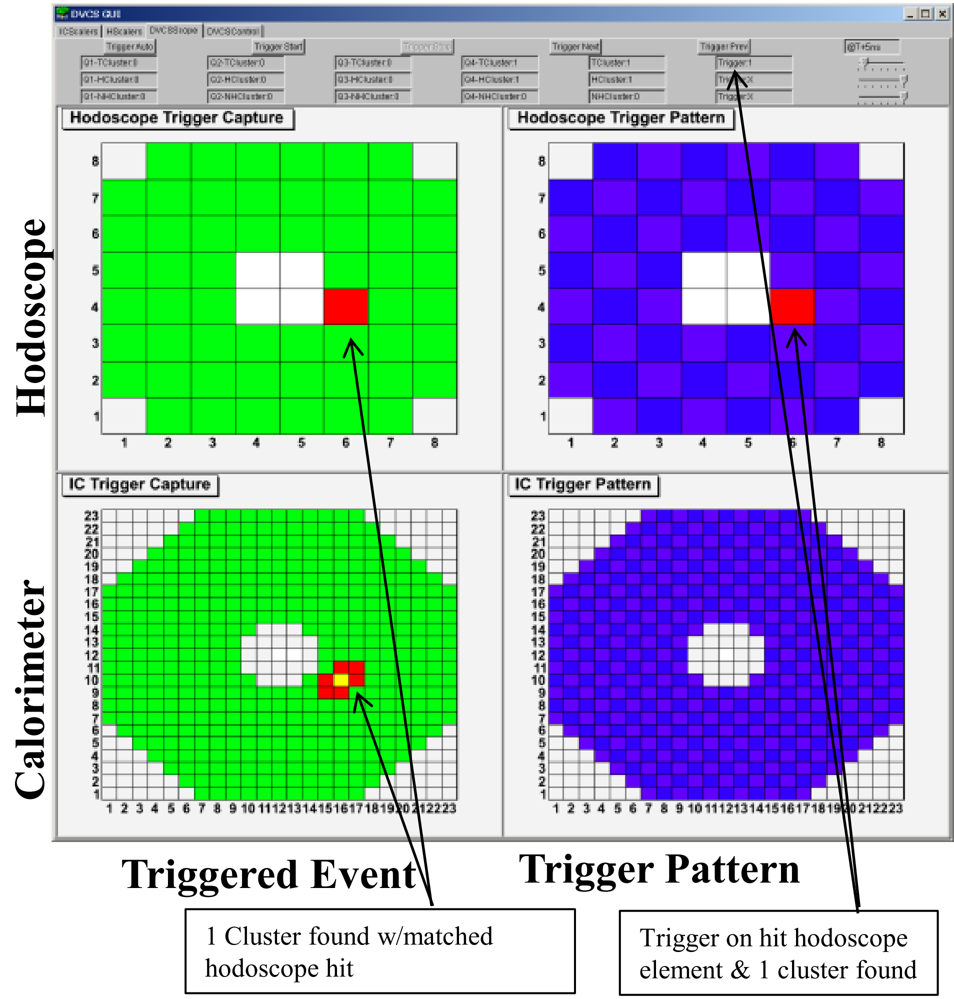
424 Tower $PbWO_4$ Calorimeter & 56 Channel Hodoscope

- FPGA based trigger finds all clusters within calorimeter by considering all possible views with a 3x3 "sliding" window

- Cluster decisions can optionally be geometrically matched with hodoscope

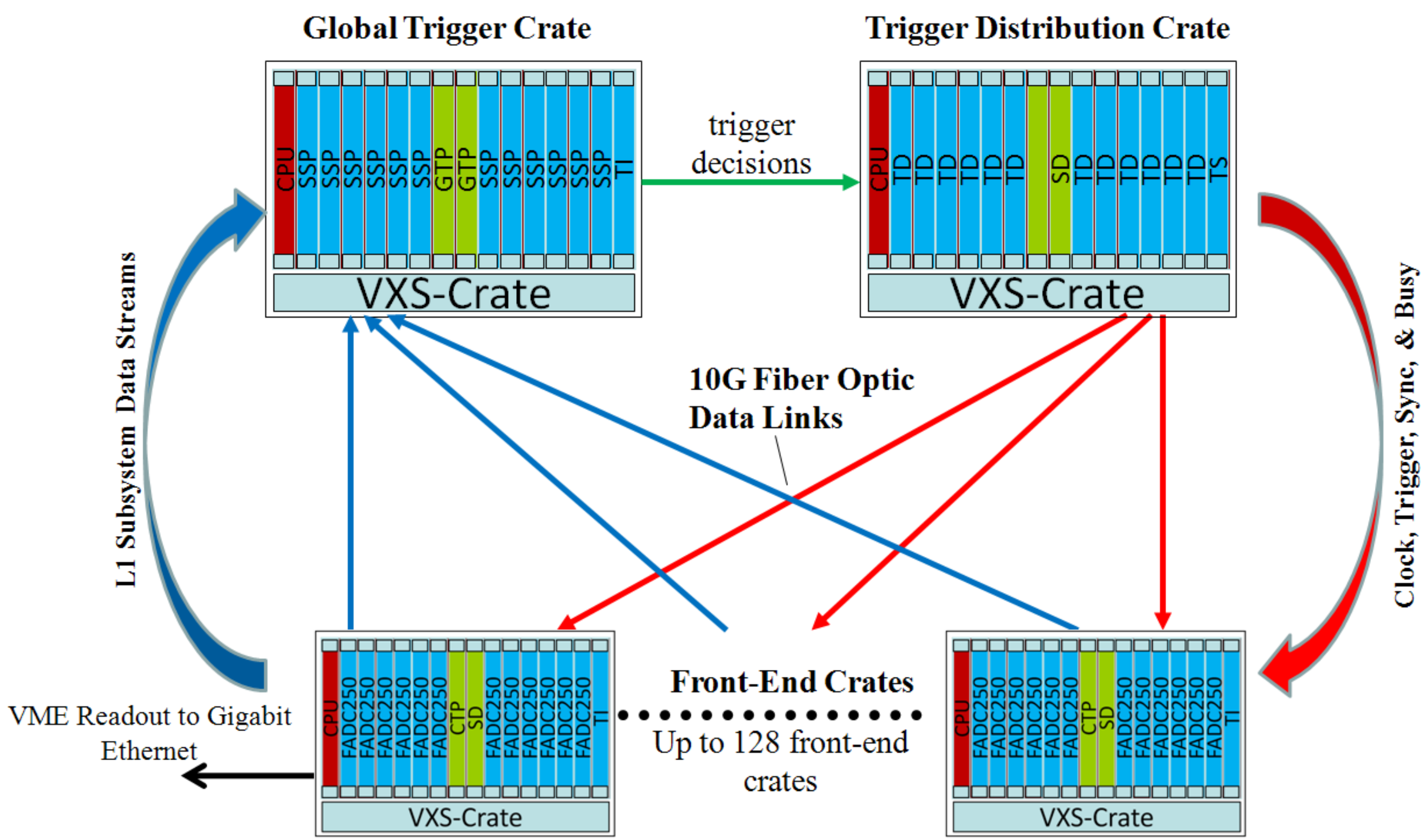
- Decision time ~85ns, 66MHz pipeline

- Trigger module has a parallel diagnostic trigger that allows arbitrary triggers to be setup for algorithm/channel/timing verification (does not interfere with data taking) ⟶

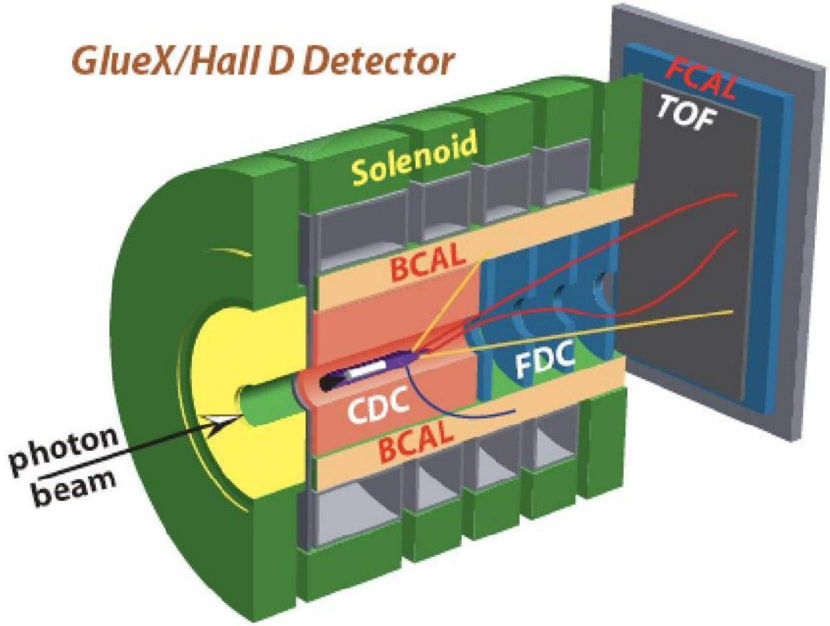


5.4 12GeV JLab Pipelined Trigger Design

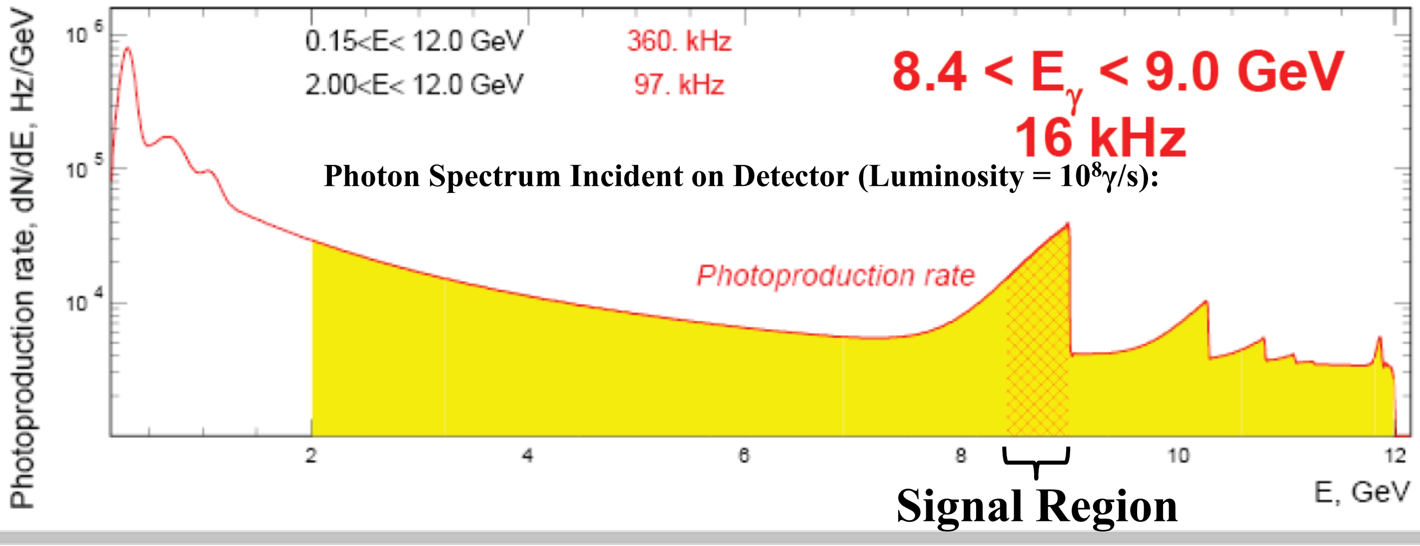
- Designed for experiments at CLAS12 & GlueX
- 125/250MHz Flash ADC based front-ends
- **>300kHz sustained trigger rate capable**
- High speed L1 trigger system (heavily based on high speed serial links & large FPGA processing)



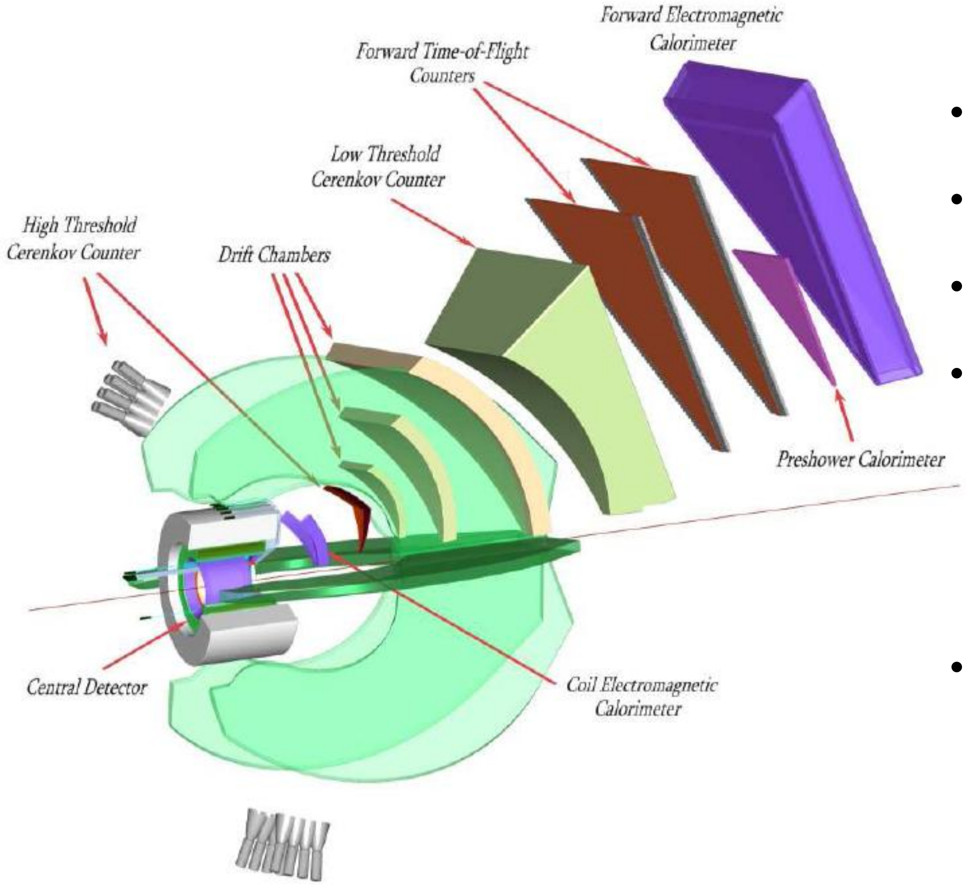
5.5 Hall D – GlueX Detector



- Photon beam experiment
- Channel count: ~22,000
- Photon Rate: $10^8 \gamma/s$
- L1 Acceptance: <200kHz
- Main L1 Trigger Algorithms
  - Energy Sums
  - Hit multiplicities
  - Low energy pulse supression
- Suppress 360kHz hadronic & 200MHz EM Background

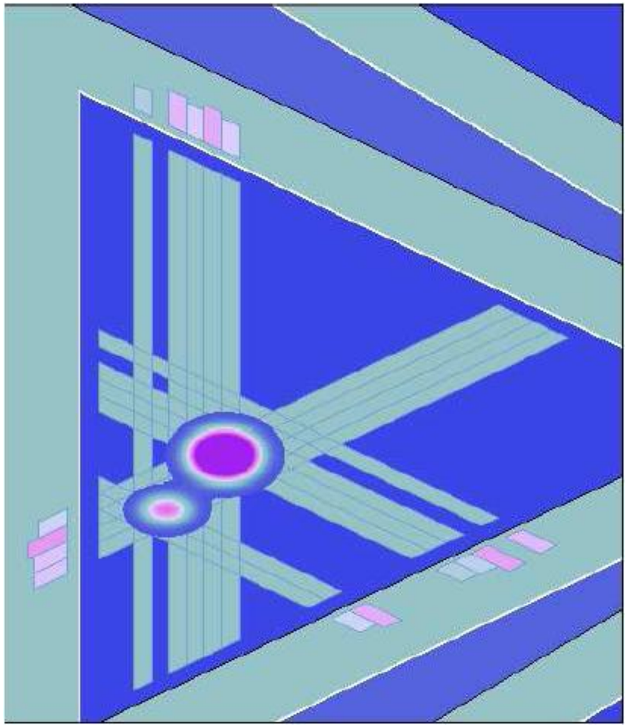


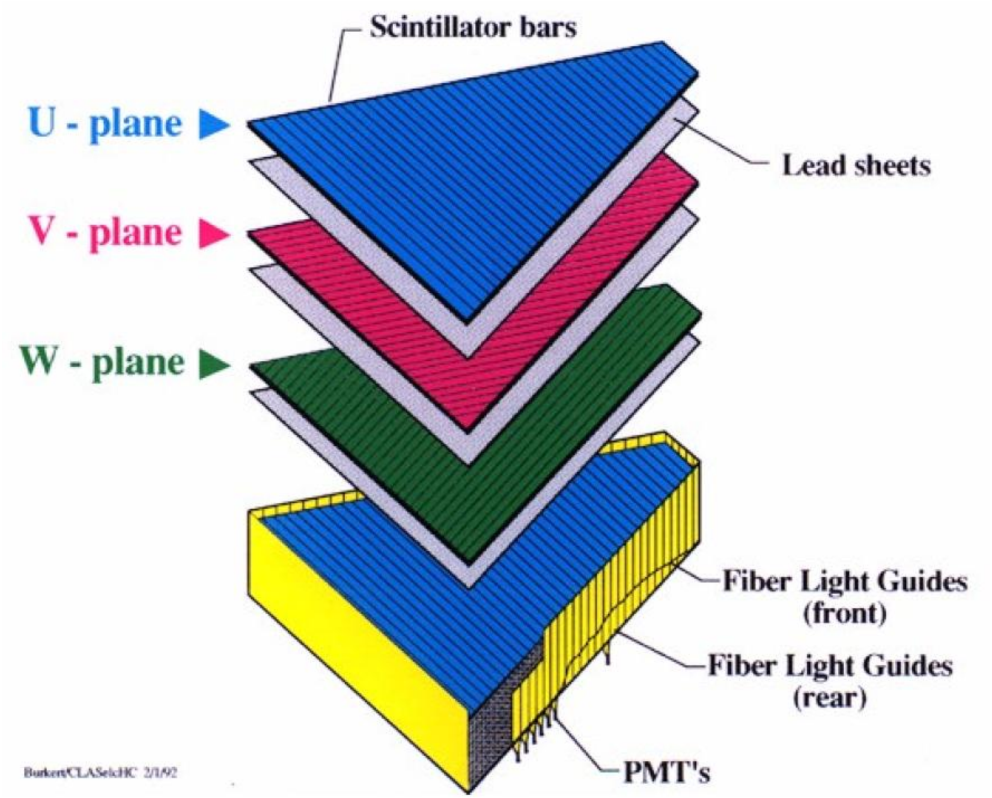
5.6 CLAS12 Trigger Design



- **Channel count:** **~40,000**
- **Luminosity:** **$\sim 10^{34} cm^{-2} s^{-1}$**
- **L1 Acceptance:** **<20kHz**
- **Main Trigger Algorithms:**
  - **EC Cluster Finding**
  - **DC Road Finding**
  - **Geometric Matching Clusters & Tracks**
- **Advanced trigger supports:**
  - **Reliable electron identification**
  - **Multi-particle events**

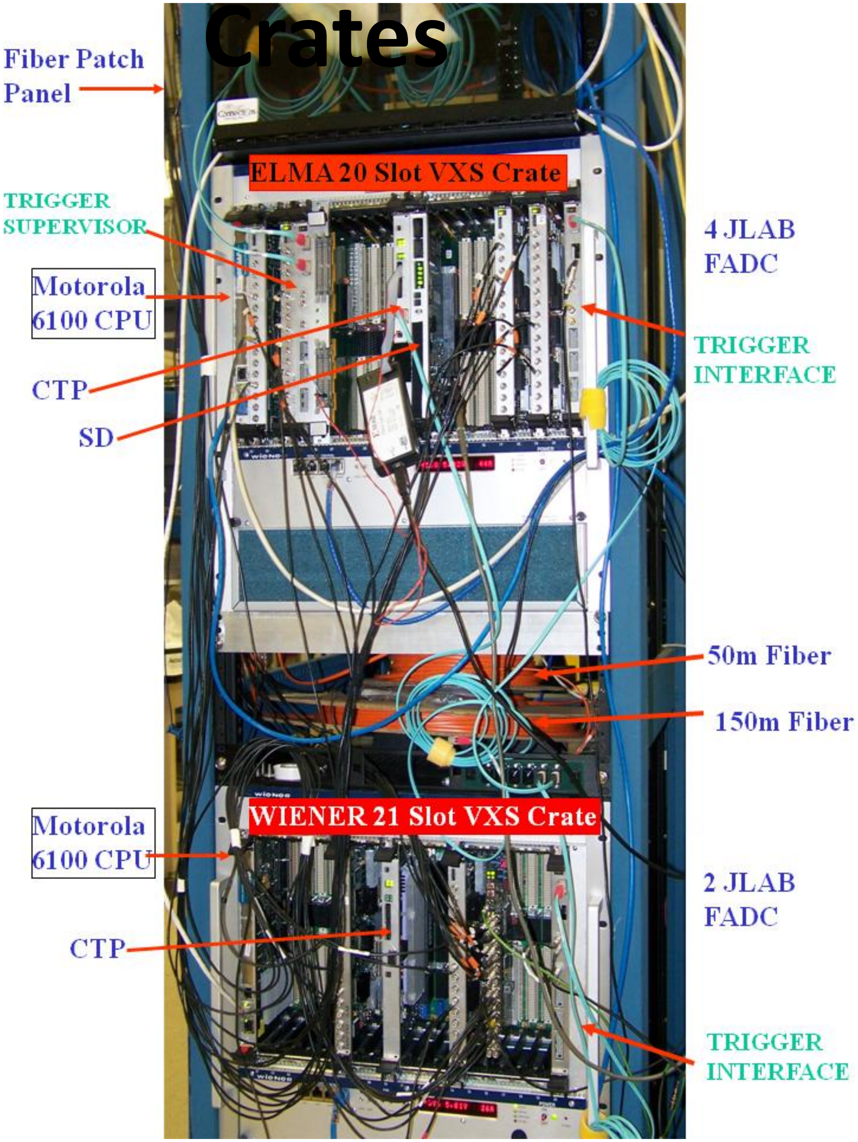
5.7 Ex: Forward Calorimeter Cluster Finding

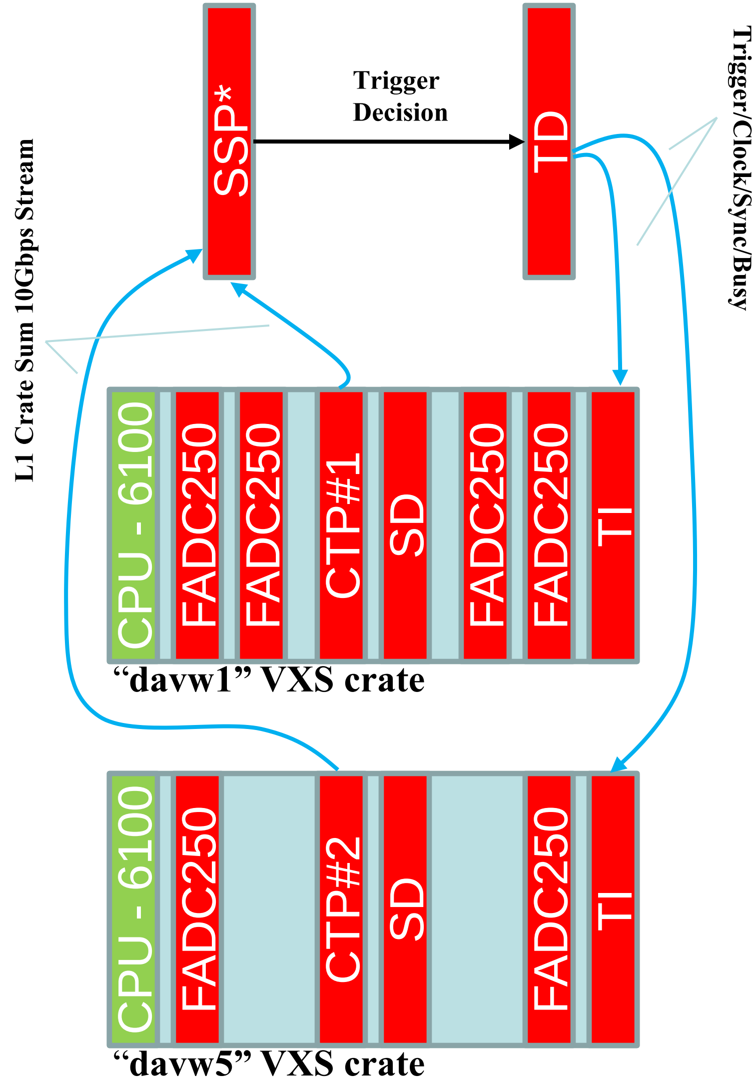




- Cluster reconstruction will be formed in L1 trigger and matched with drift chamber tracks on a per sector basis.

5.8 2 Fully Prototyped Front-End Crates





*SSP function embedded inside 2nd CTP

In Conclusion…

- EIC Triggering will need a modern trigger system & DAQ to support high trigger rates and suppress background events

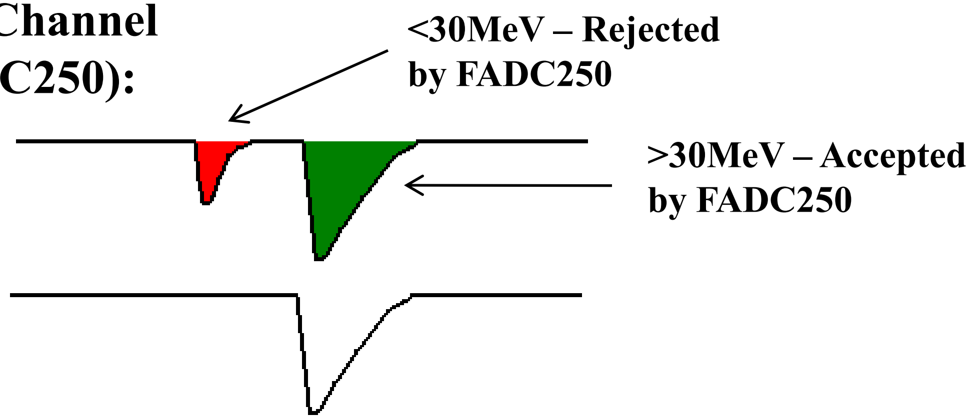
- JLab 6GeV experience and 12GeV development address many issues surrounding high speed trigger development & advanced trigger support

GlueX Example L1 Trigger

BCAL & FCAL <30MeV Channel Suppression (done at FADC250):

FADC Channel Input:

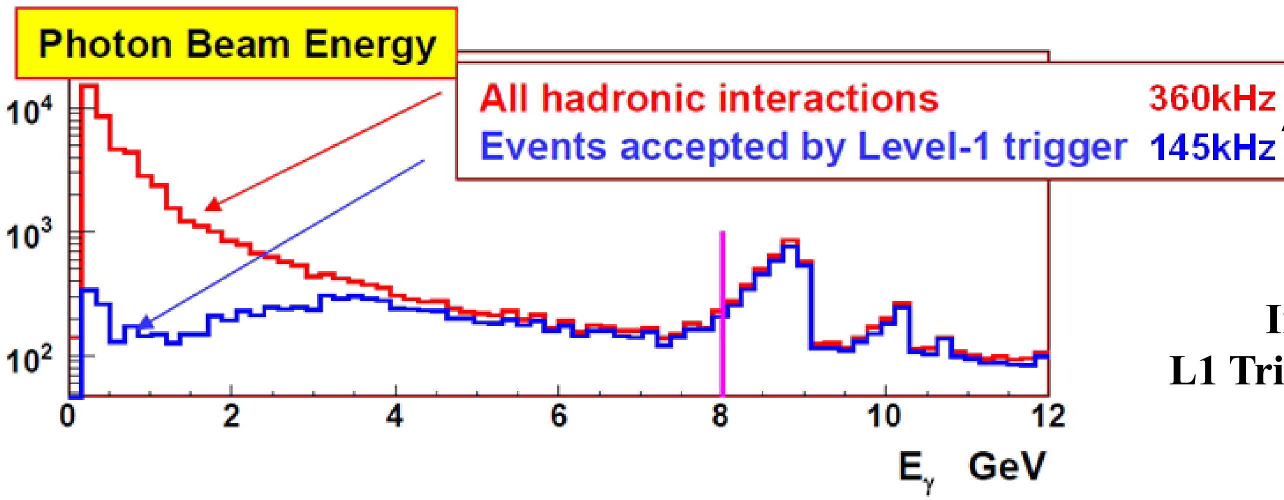
FADC L1 Sum Output:



GTP Trigger Equation:

$$\sum_{t}^{t+100ns} ST_{hits} > 0 \quad \&\& \quad \sum_{t}^{t+100ns} BCAL_{energy} + 4 * FCAL_{energy} > 2GeV$$

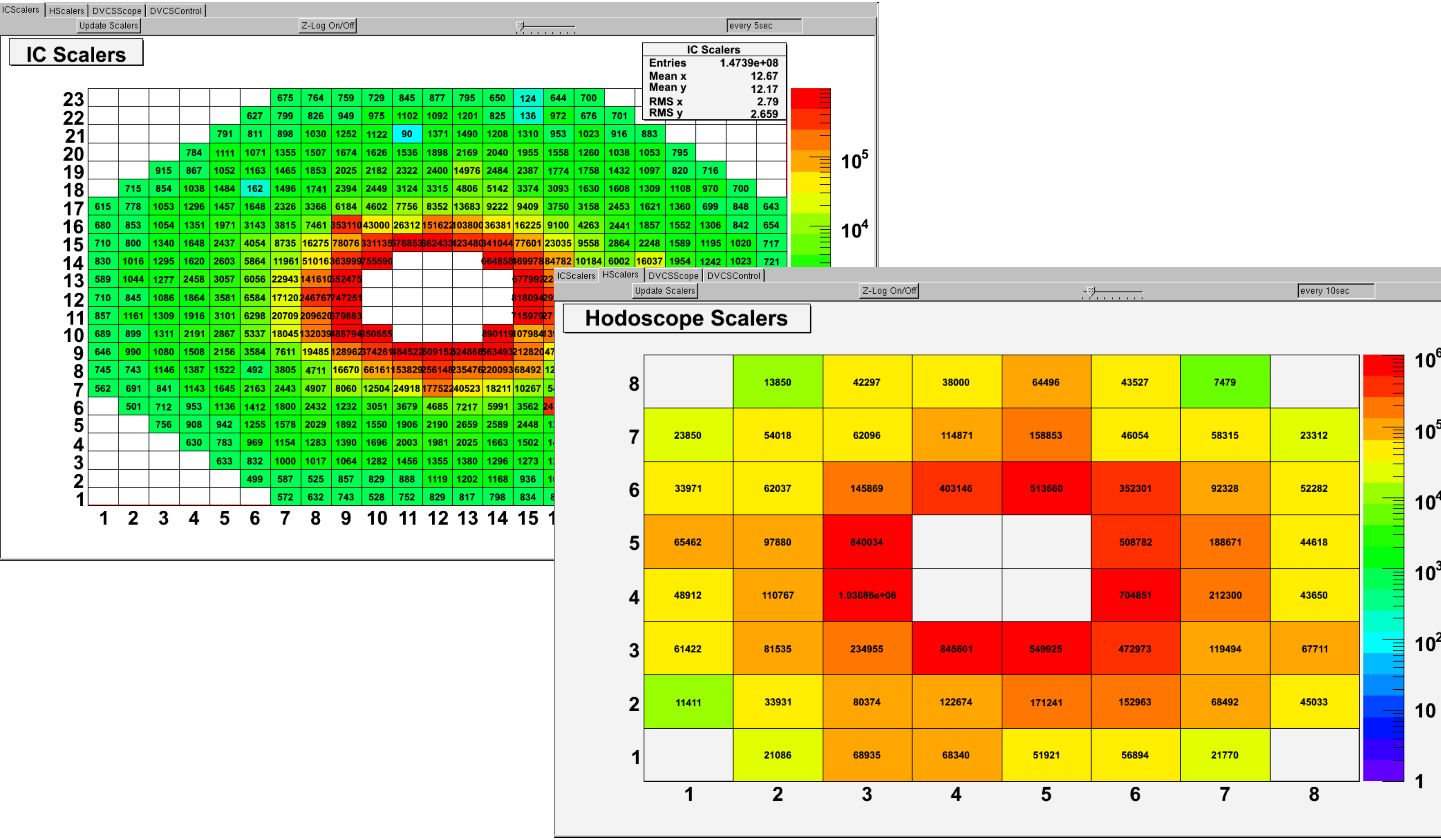
Resulting L1 Acceptance Spectrum:



L1 Rate < 200kHz

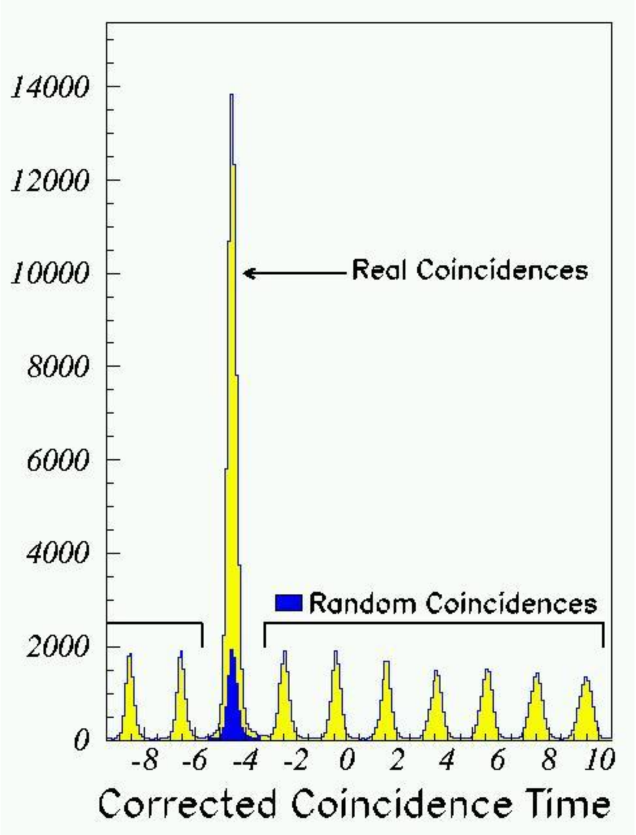
In Signal Region:
L1 Trigger Efficiency > 92%

IC & Hodoscope Trigger Logic

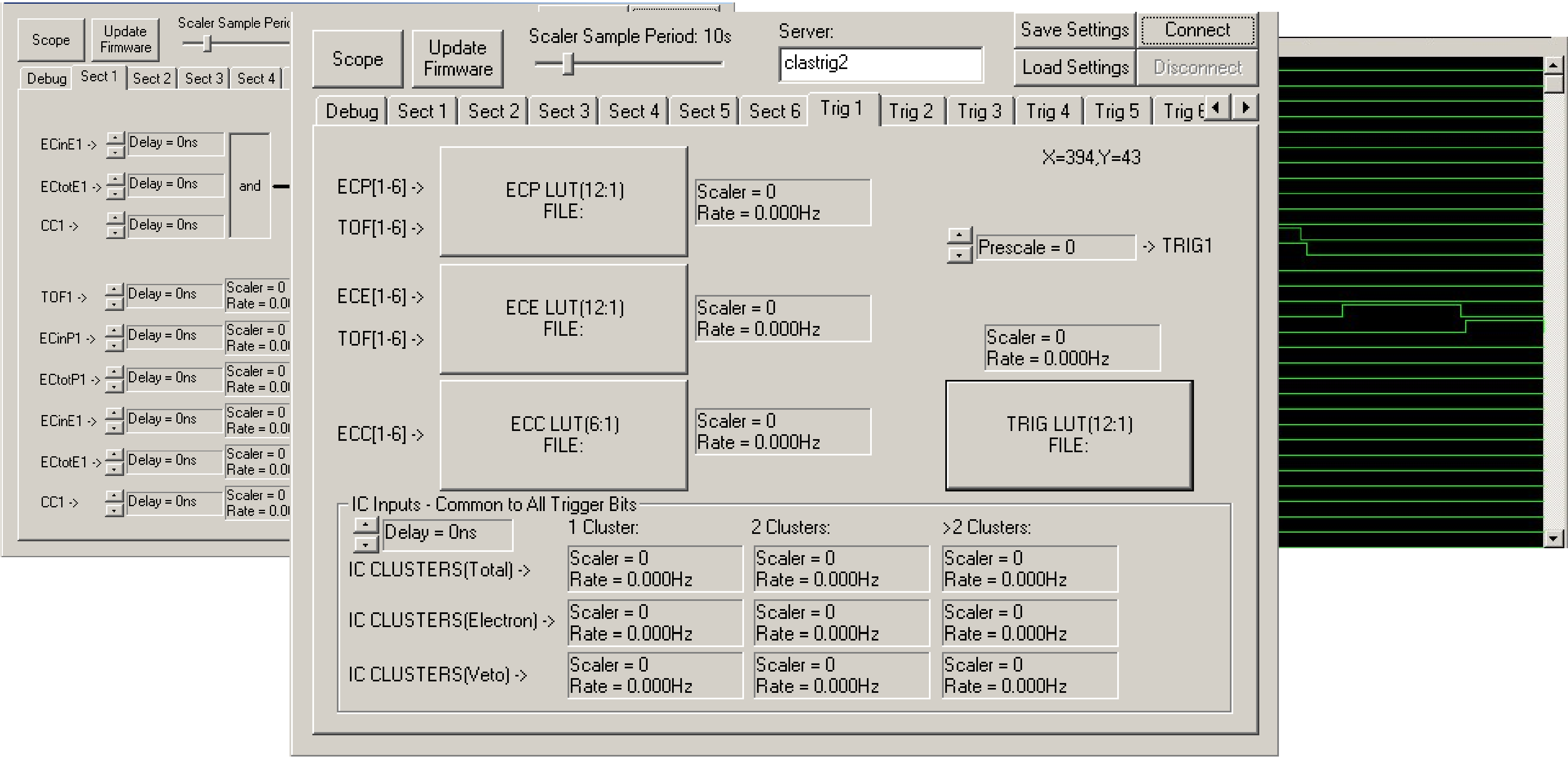


Event Trigger

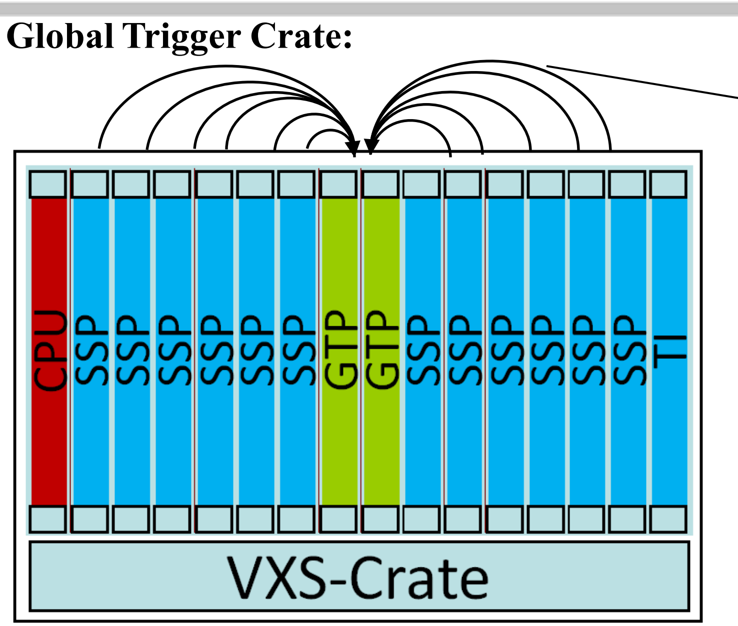
- A trigger condition will create a signal sent to all front-end modules to “readout” the event
- Timing resolution of event is resolved using high resolution TDCs and timing information received from ADC modules
- Triggered window/integration gate widths are much large than the bunch crossing time, so event data corresponds to multiple bunch crossings. Real event bunch crossing is easily distinguishable because of high resolution timing information
- CW beam creates random background which can be used to correct real event statistics



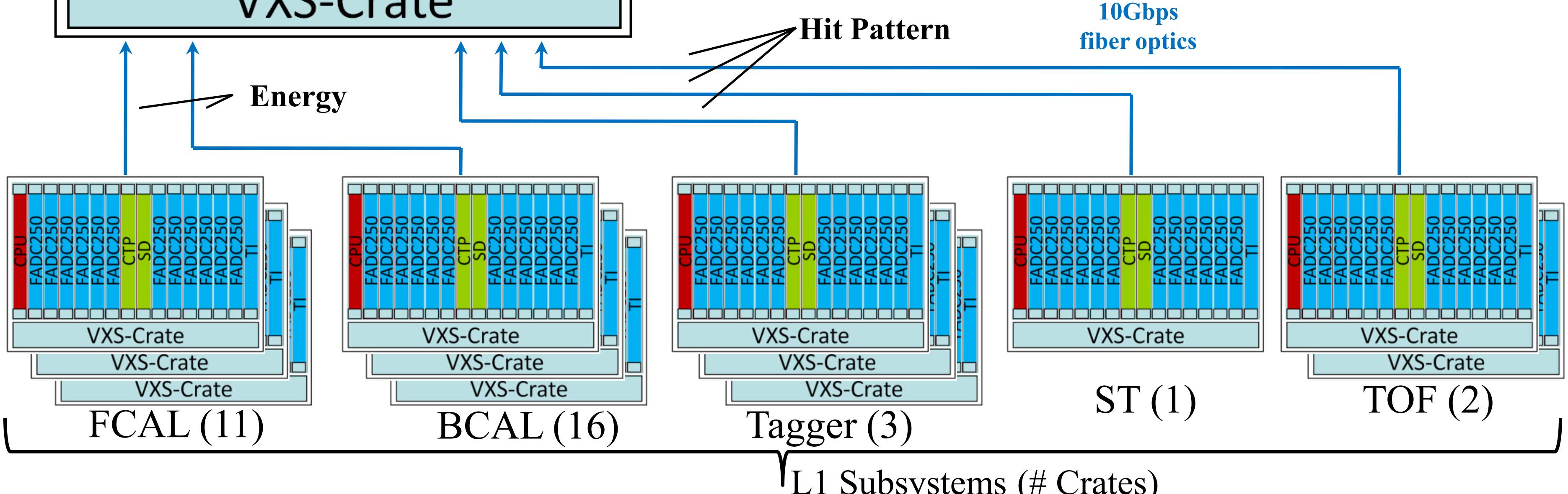
Global Trigger Logic



GlueX Trigger Subsystems



- Sub-System-Processor (SSP) consolidates multiple crate subsystems & report final subsystem quantity to Global-Trigger-Processor (GTP)
- 32bit quantity every 4ns



5.2 Existing CLAS Trigger