



Ethernet Based Embedded System for FEL Diagnostics and Controls

J. Yan, D. Sexton, A. Grippo, W. Moore, and K. Jordan

FEL, Jefferson Lab

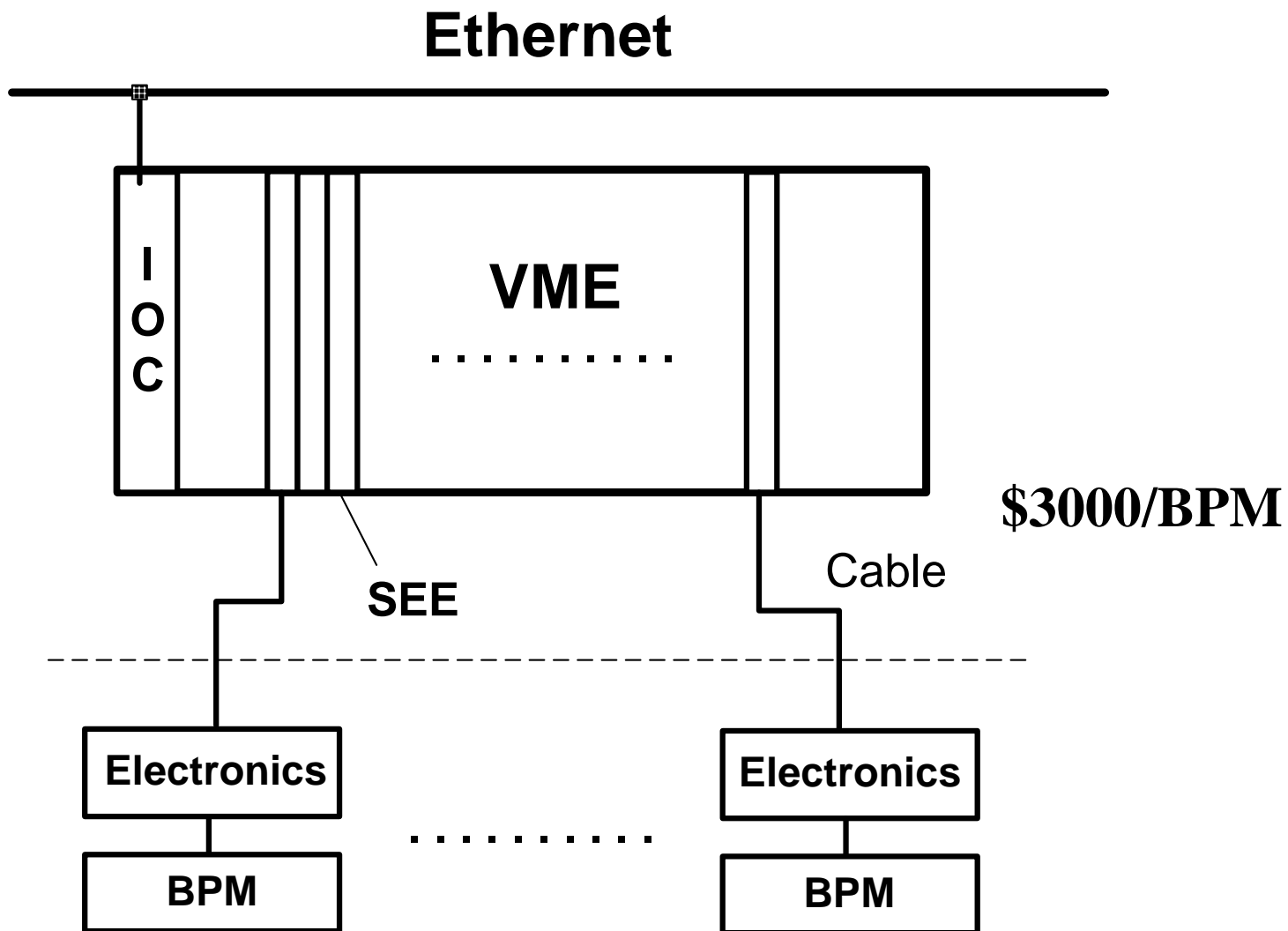
Oct. 2006

PCaPAC 2006

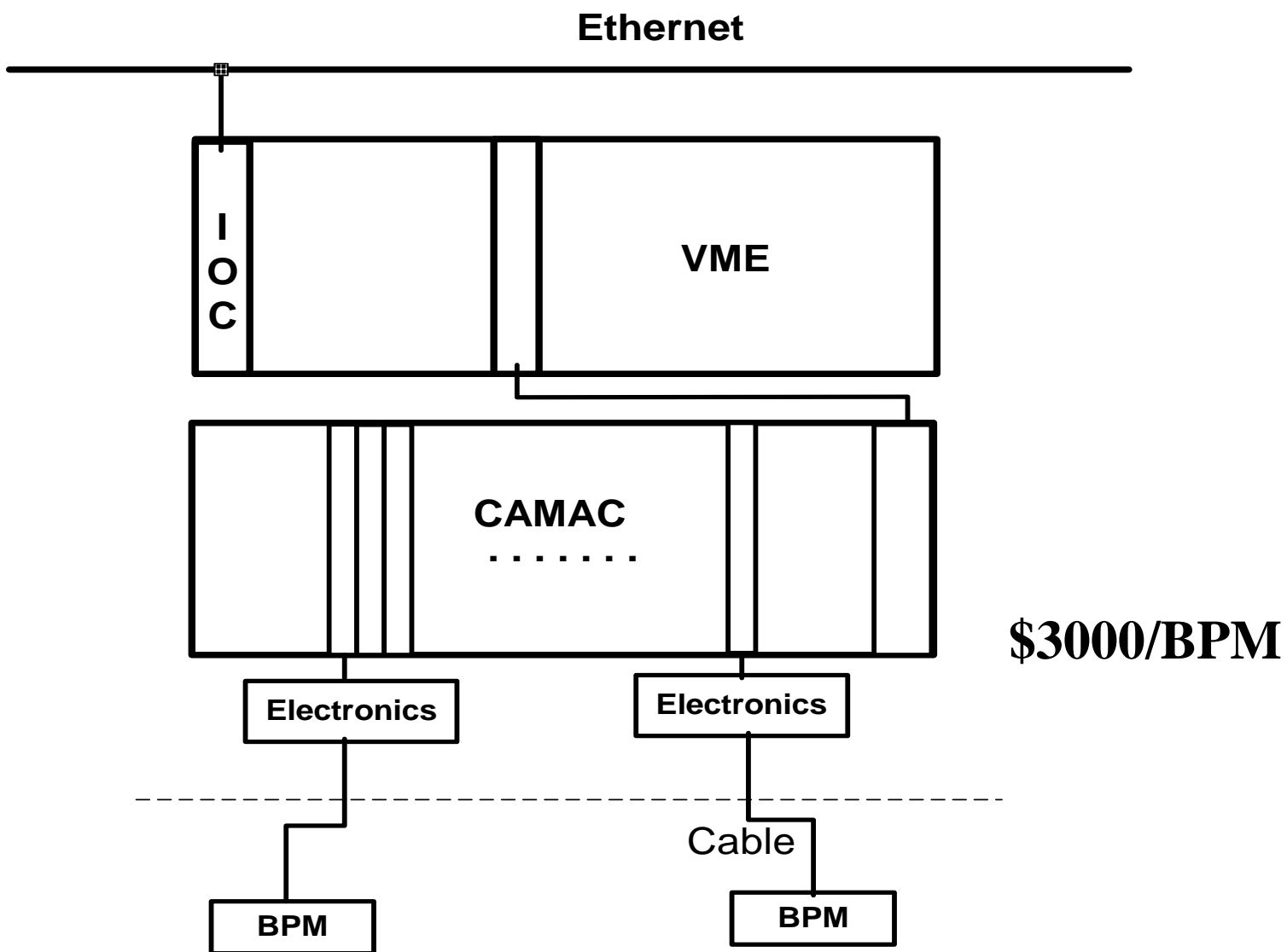
Motivation

- FEL requirements for additional channels of BeamViewers and BPMs
- The cost for expanding the current configuration is high
- FEL “master plan” is to move away from Crate-Based solutions involving licensed software
- Use distributed processors instead of VME IOCs
- Develop a new I/O connection as a “default” standard
- Embedded Arcturus Coldfire Board chosen to start with
- Chose RTEMS as the real-time operating system for the IOC

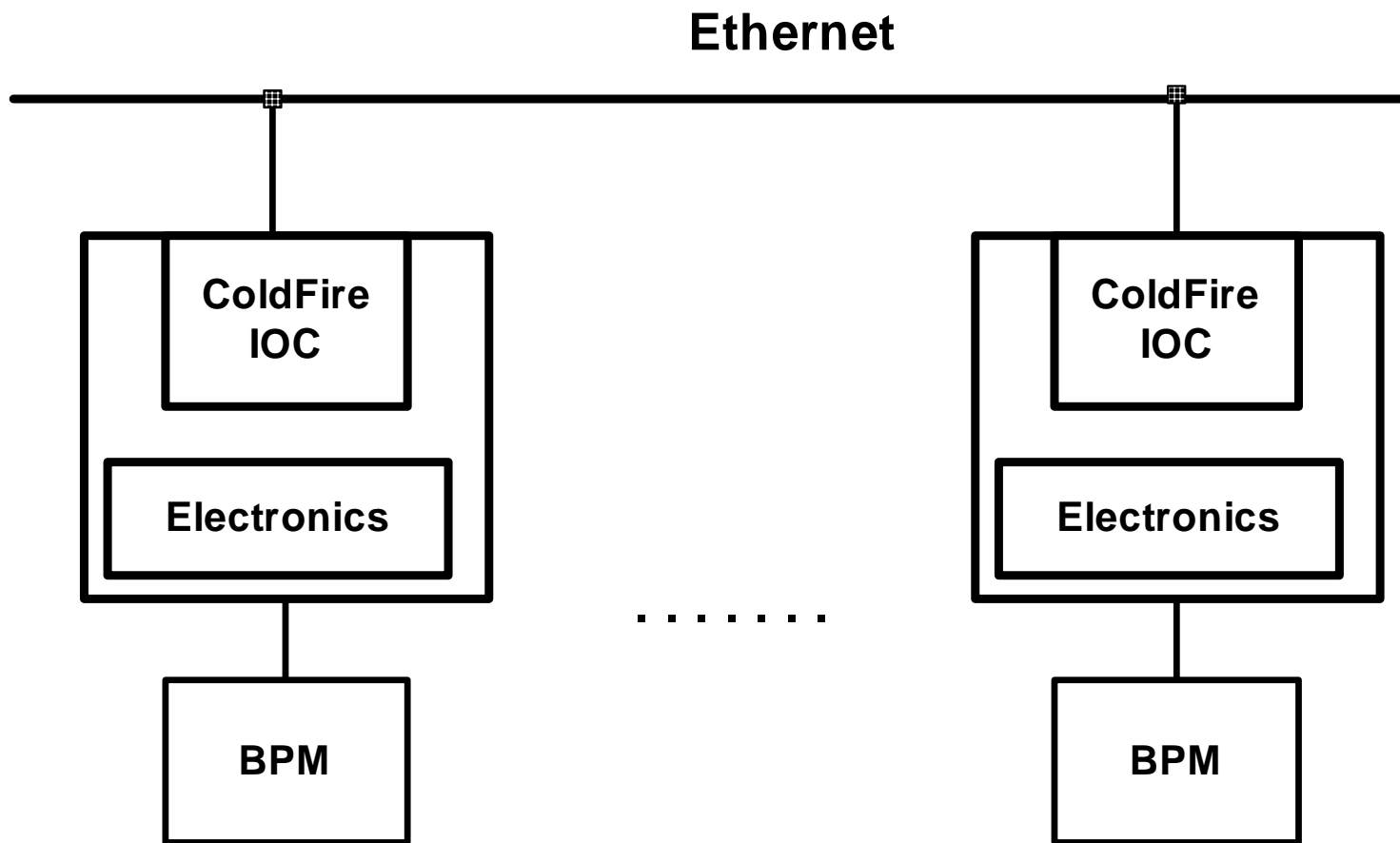
Current BPM Configuration 1



Current BPM Configuration 2

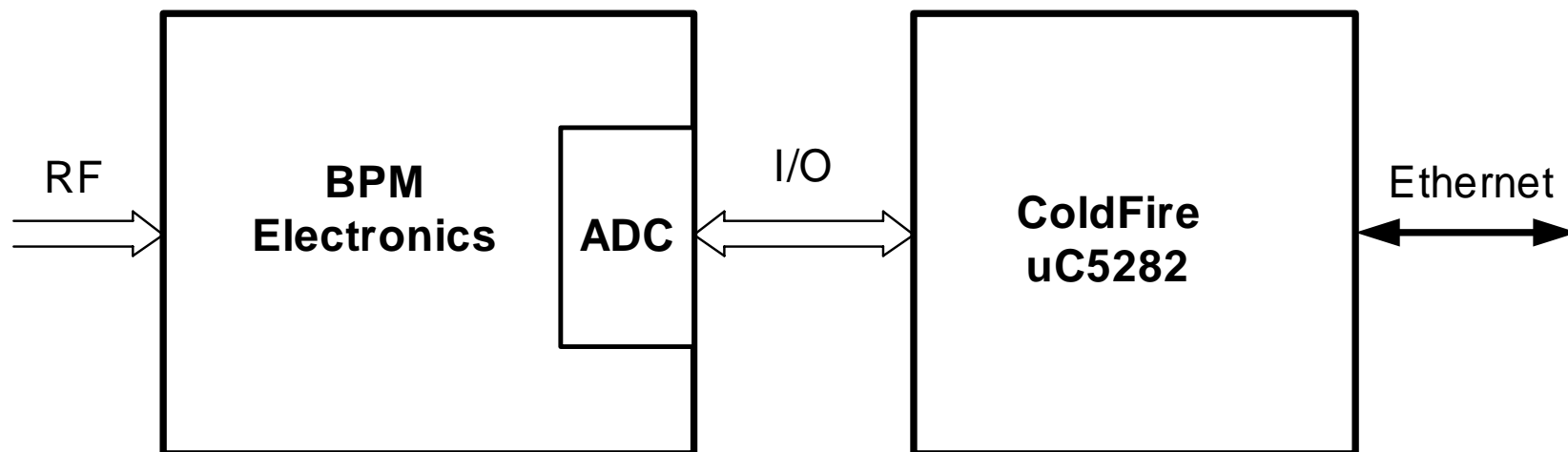


New BPM Configuration- Based on Embedded IOC

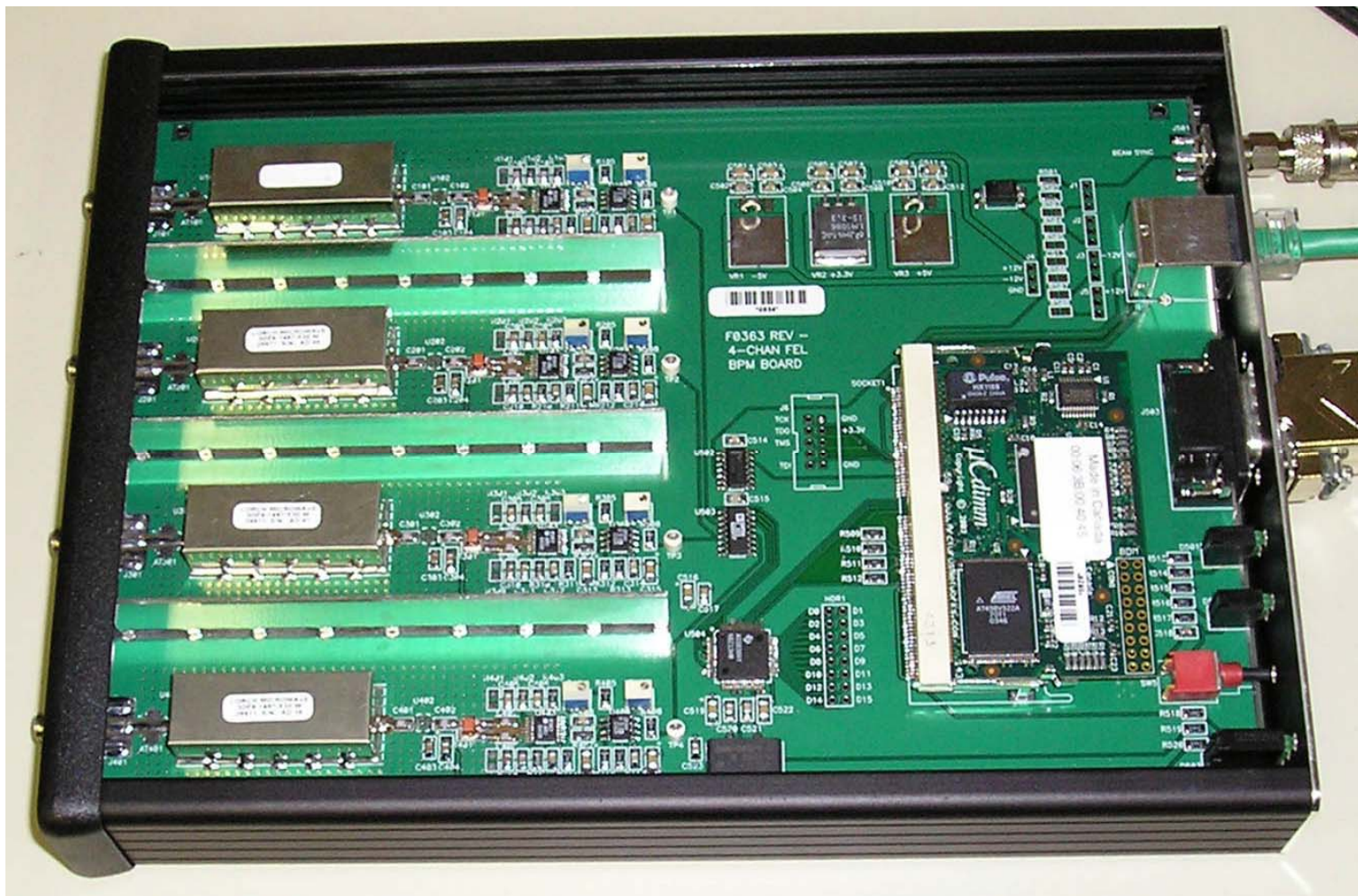


\$750/BPM

BPM Schematic



BPM Board



Embedded Processor – ColdFire 5282 (uC5282)

- “System on a module”
 - Core processor, memory, Ethernet
- Hardware features
 - 16 MB RAM
 - 10/100 Ethernet support
 - Two RS232 serial ports
 - CAN 2.0 Bus
 - QADC
 - QSPI
 - Timer Module
 - I2C bus controller
 - Many GPI/O pins



Software

- **Bootloader**
 - Load the operation system
 - Set the boot environment(IP, server, startup script)
- **RTEMS**
 - Real-Time Operating System for Multiprocessor Systems
 - Open source
 - Open development environment
 - Cross development with EPICS (3.14)

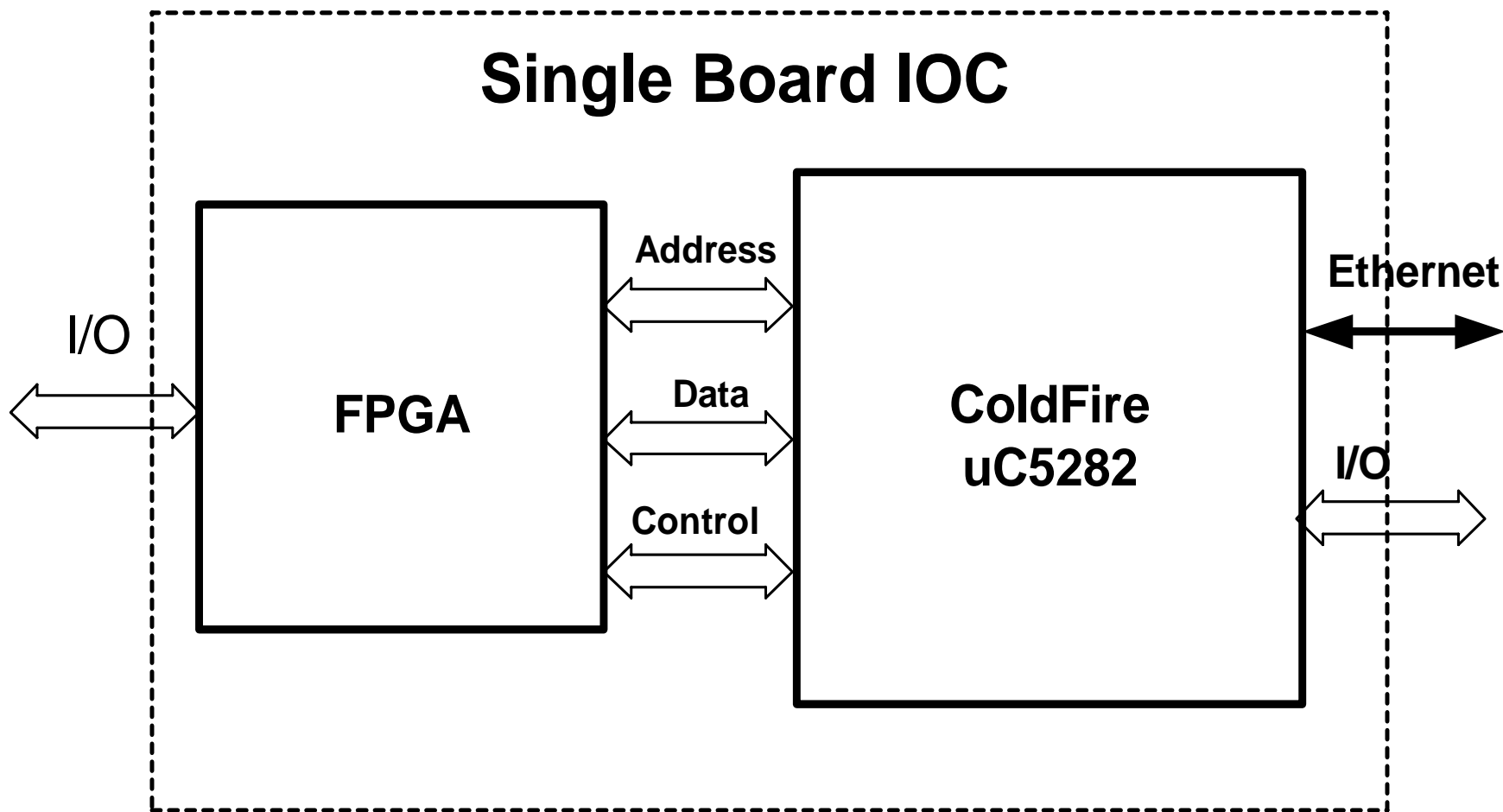
IOC Applications

- **Install RTEMS**
 - /usr/local/rtems/rtems-4.7
- **Install EPICS**
 - Version base-R3-14
- **Make the Application**
 - makeBaseApp.pl
- **Develop the Application**
 - Device driver, device support, Sequencer, database
 - Remote programming, remote reboot

Result of the BPM

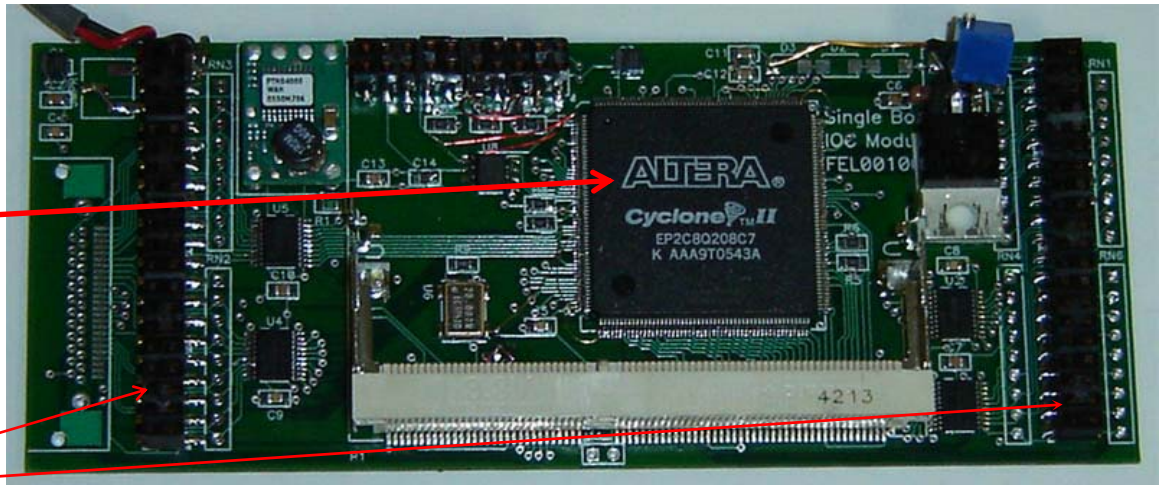
- The first version of new BPMs have been running for over 1 year
- They are very reliable, and easily maintained
- Throughput from the ADC is 100 Hz. This is a limitation
- New solutions have to be found
- Develop a “default” standard for the new I/O connection
- New configuration -- **Single Board IOC**

Single Board IOC



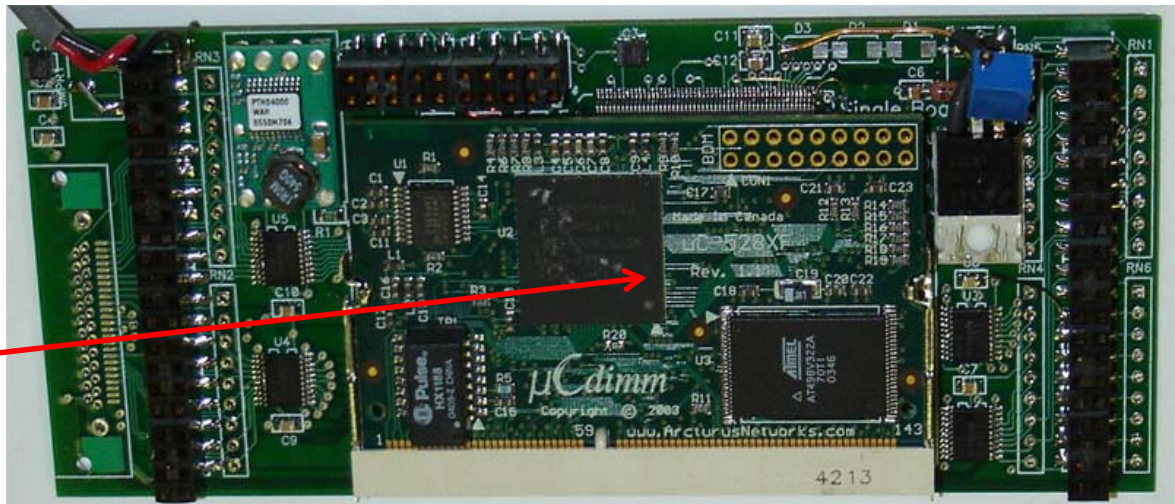
Pictures of SBIOC

FPGA



40 Pin Header

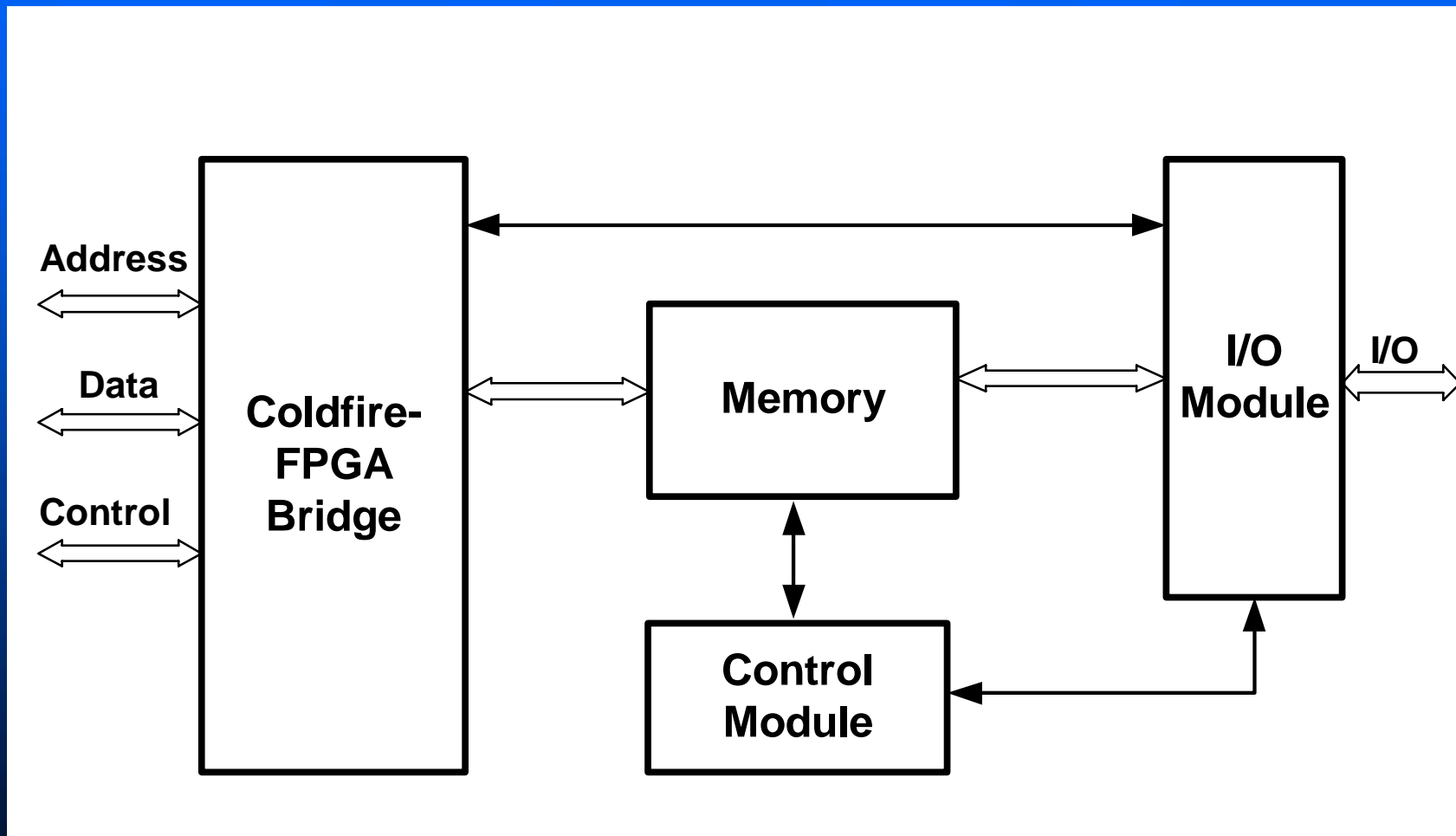
uC5282 Processor



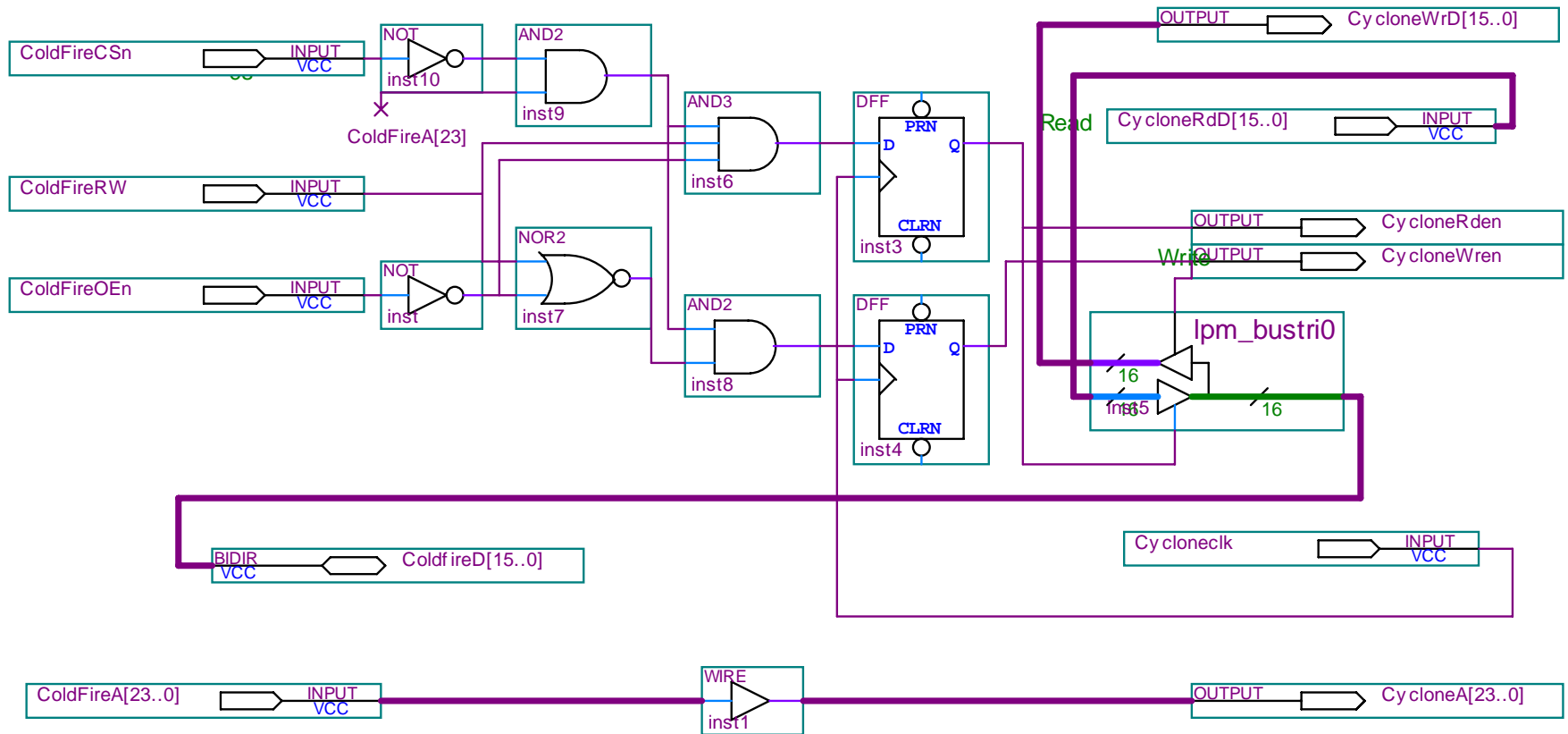
FPGA

- ALTERA Cyclone II EP2C8Q208C7
- Low cost (\$20.30), high Volume (8,256 Logic elements)
- 208-pin PQFP, easy to solder
- Easy programming
- Use Quartus II 5.1 software
- Support AHDL, VHDL, Verilog HDL, Block Diagram/Schematic files
- Code downloaded in an EPROM

Functionality Modules of FPGA



Circuit of the Bridge



The New BPM

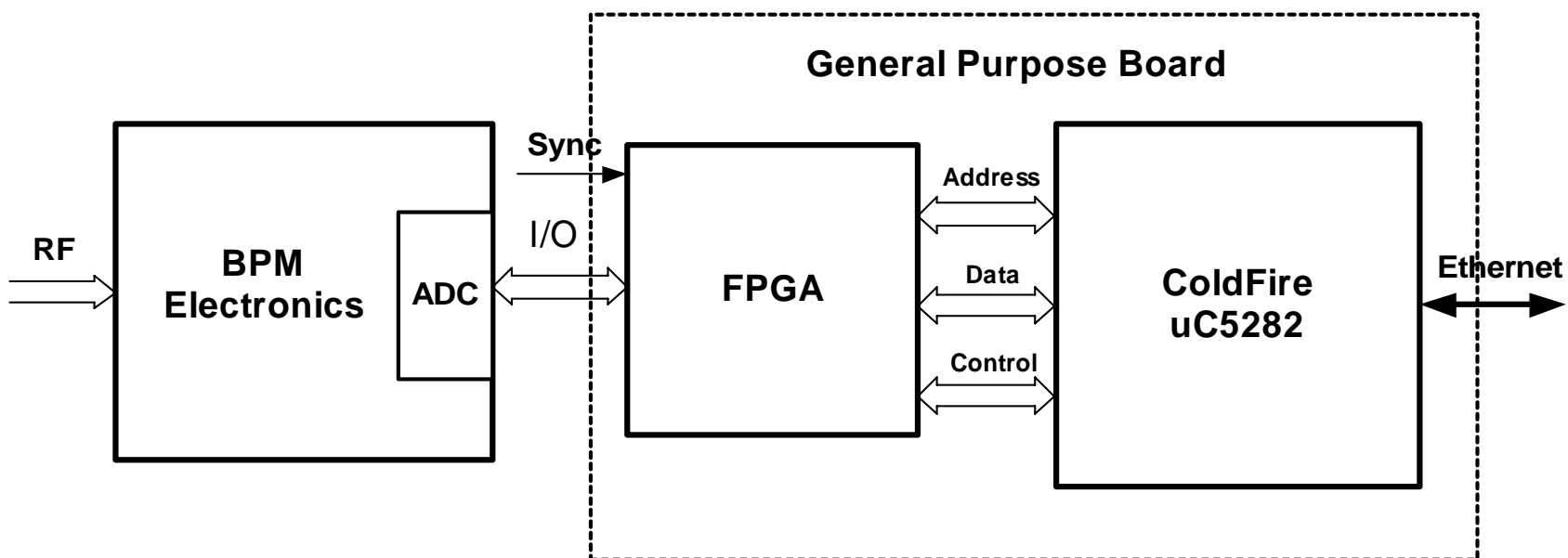
* FPGA Functions:

- Sampling ADC, Calculations (add & average)
- Communication with ColdFire

* Goal: 300KHz Throughput

- FPGA clock 20 MHz
- ADC 500 KHz
- FPGA sampling frequency 1 MHz
- Memory block to save data
- Coldfire processor read data through bus

New BPM Schematic



Applications of SBIOC

- The Single Board IOC will be used for most of I/O control in FEL.
- There are some other systems going to be upgraded with the SBIOC
 - Beam viewer crate, GC chassis, Charge/Dump chassis, Vacuum crate,...
 - A General Purpose Board as a carrier board is designed, and it is pin-pin compatible with preexisting cards.

Summary & Conclusions

- The first version of BPM based on embedded IOC had been running on FEL. It is reliable, and easily maintained.
- Setup the software
 - EPICS, RTEMS, Device support, Database
 - Startup (boot) procedure
- Designed the Single Board IOC
- ColdFire uC5282 processor is an ideal choice for the embedded IOC
- Use RTEMS as the real-time operating system
- By distributing the IOC on front-end I/O devices, dramatically cut the cost of expensive cables.
- It is a novel configuration to use FPGA+uC5282+RTEMS for FEL diagnostics and controls upgrading

Acknowledgement

■ Thanks

- Eric Norum in Argonne National Lab for providing RTEMS tools and the step-by-step installation instructions.
- Steve Dutton for electronics board making
- Trent Allison in ESICS group of Jefferson Lab for the help of Altera FPGA programming.
- The Operations and Commissioning team of the FEL for the support and technical advice

- This work is supported by the Office of Naval Research, the Joint Technology Office, The Commonwealth of Virginia, the Army Night Vision Laboratory, the Air Force Research Laboratory, and by DOE Contract DE-AC05-84ER40150.