

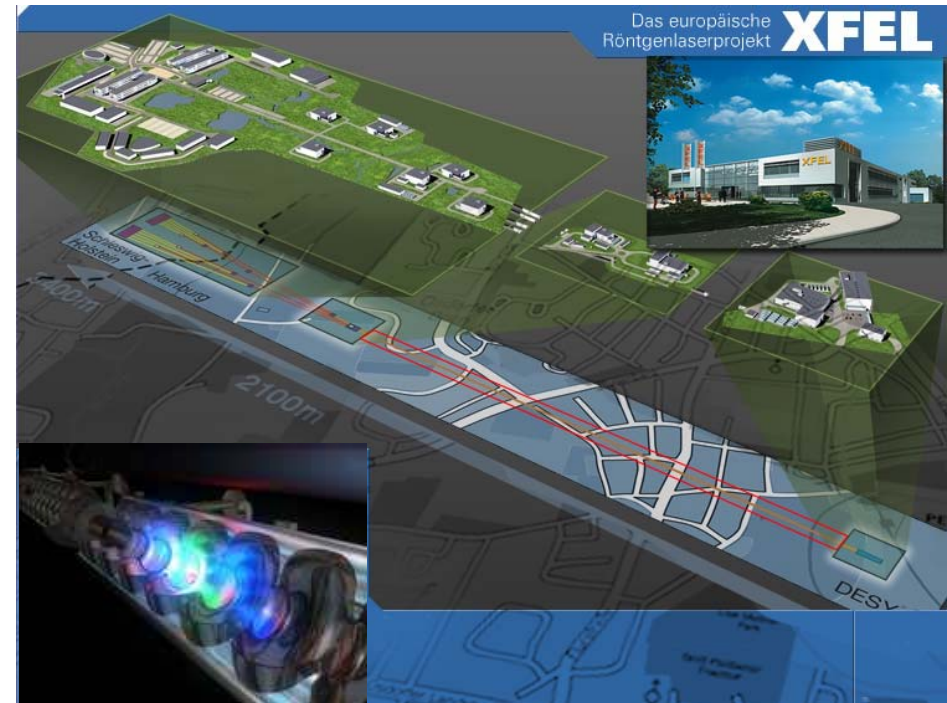
# **A configurable Interlock System for RF- Stations at XFEL**

*M.Penno, T. Grevsmühl, H.Leich, A. Kretzschmann  
W.Köhler, B. Petrosyan, G.Trowitzsch, R.Wenndorff*



- XFEL Project
- Interlock Concept
- Interlock Hardware
- Software for the Interlock

- *XFEL* → *European X-ray free-electron laser project*
- opens many possibilities for research with short wave length x-rays (below 1 nm)
- start of construction 2007
- initial operation 2012
- requires 33 ... 40 RF-Stations for the accelerator sections based on super-conducting cavities





- Interlock Concept
- Interlock Hardware
- Software for the Interlock

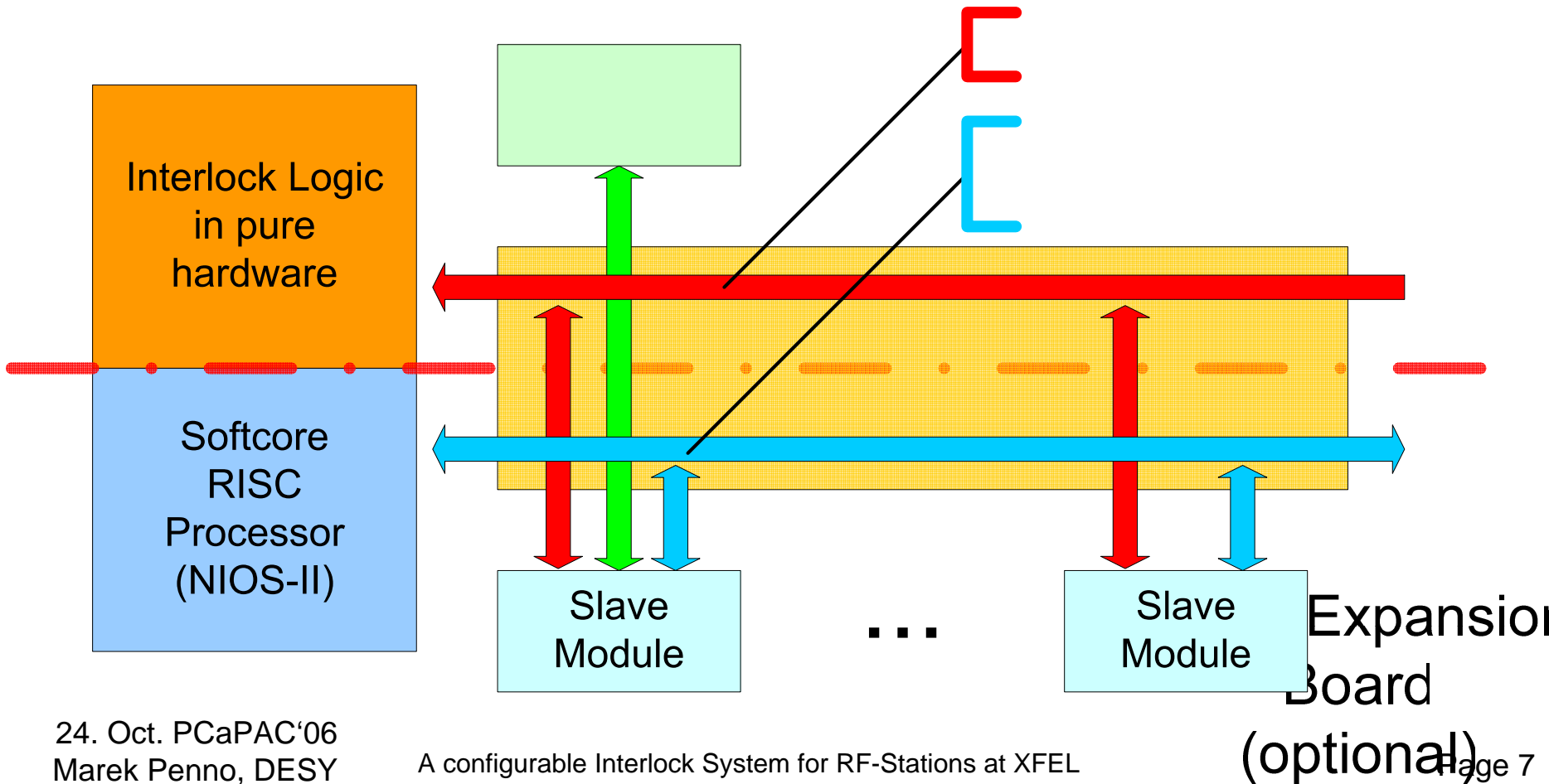


- Guarantee operator's & other person's safety
- Prevent any damage from the cost expensive components of the RF-Station
- Prevent also any damage from other equipment

- Hardware failures (non-reversible malfunctions)
  - broken cable or damaged contact, dead sensor, ...
- Soft errors (reversible error conditions)
  - sparks in the klystron or wave guide system
  - temperature outside a valid range, ...
- Error conditions caused by transient noise from the RF-Station itself

# Interlock architecture overview

- interlock function completely implemented in hardware
- **Strict** separation of interlock logic and processor bus





- Interlock Concept
- **Interlock Hardware**
- Software for the Interlock



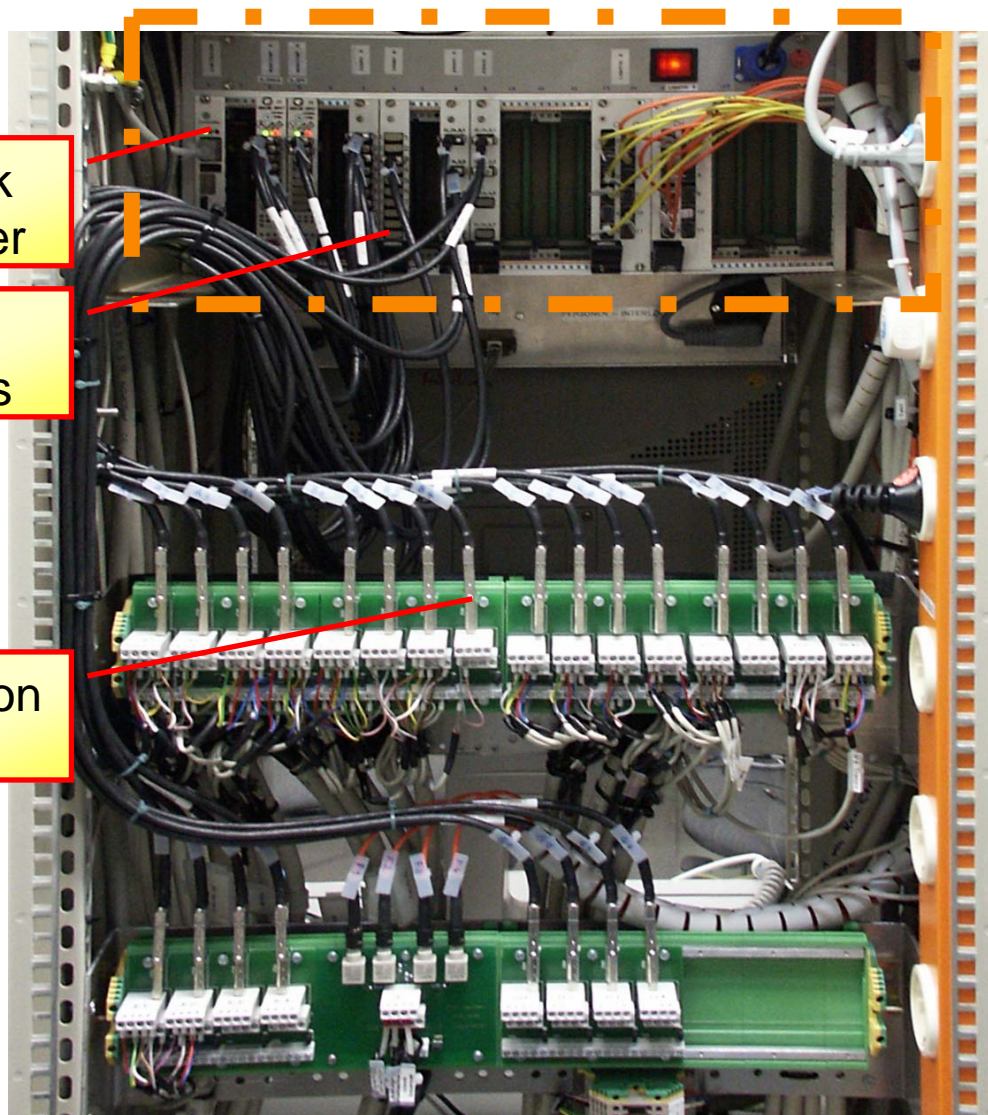
# Interlock Crate

- 19`` 3HU crate
- 20 slots for slave modules
- provides many signal connections
- distribution panels connect the interlock crate with incoming and outgoing signal cables
- easy access to all signal cables
- easy module exchange

Interlock  
Controller

Slave  
Modules

Distribution  
Panels



# Interlock Modules





- 😊 easy scaleable by *Altera SOPC-Builder*
- 😊 good IDE integration and development flow
- 😊 close to hardware development
- 😞 no Memory Management Unit (*MMU*)
  - not suitable for our software project
  - software errors hard to find
- 😞 strange behavior with LWIP-Stack and  $\mu$ C/OS on our board
- 😞 fixing errors often very time consuming

# Planned future development

- move on-board applications from NIOS/II to another platform
- shrink on-board applications on NIOS/II side
- mount computer-on-board module on controller (f.ex. X86-architecture, X-Board)
- use Linux as operating system



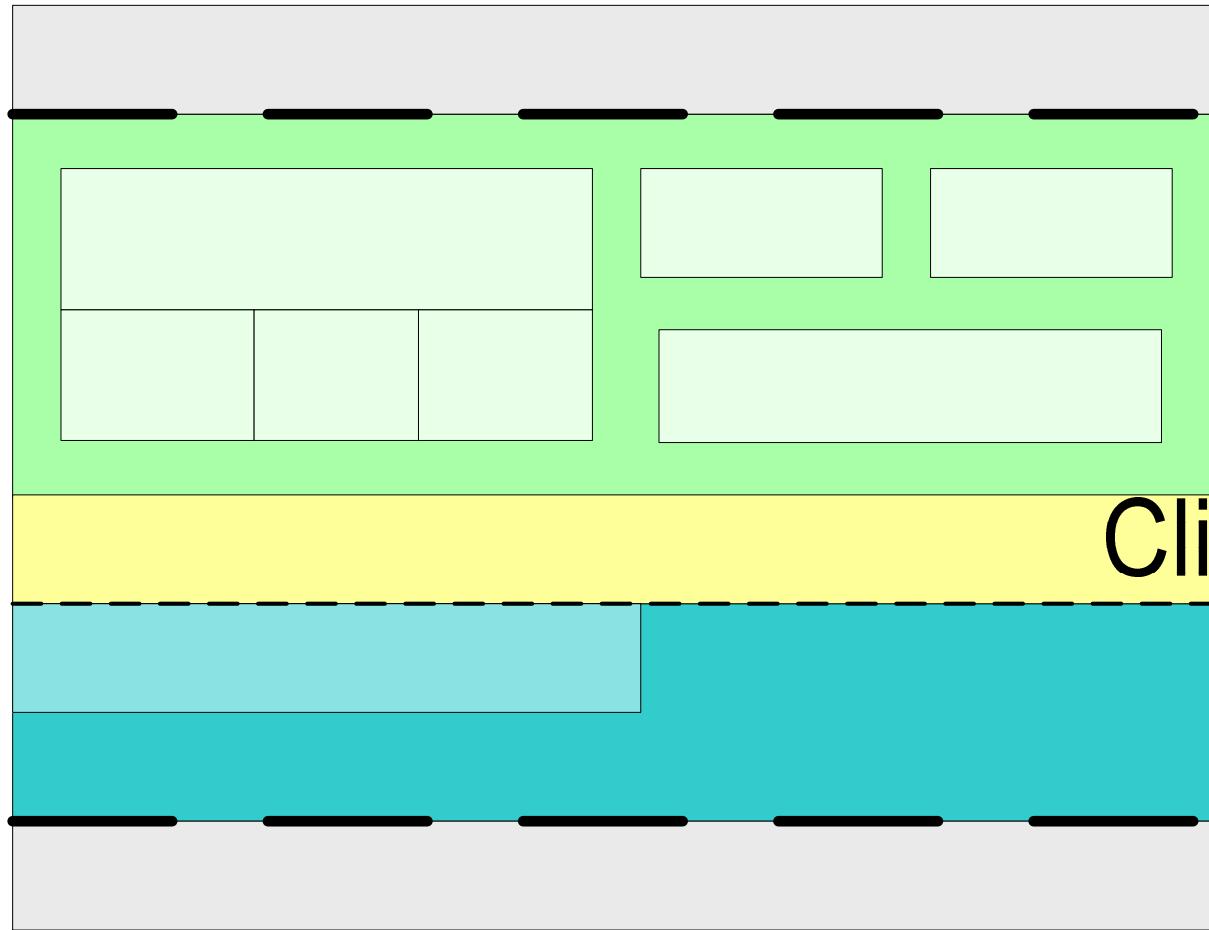
- AMD Geode SC1200 CPU 266 MHz
- Up to 128MB RAM / 128MB Flash on board
- Integrated video controller with up to 4MB DRAM
- Power consumption 3-4Watts
- On board 10/100MBit Ethernet
- IDE interface with UDMA-33 support
- PCI and LPC expansion busses
- 3 USB 1.1 ports OHCI
- 2 serial interfaces (TTL signals)



- Interlock Concept
- Interlock Hardware
- **Software for the Interlock**

- Perform several tests at power-up (System-Selftest)
- Accessed over intranet via browser
- secured access by user authentication
- Display signal status and change signal mask
- Special mode for updating firmware and FPGA design

# Klystron Interlock Server - Architecture



Client application

UDP I  
to DC

# System-test on power-up

- System-selftest runs on power-up
- System-selftest steps:
  1. controller
  2. backplane
  3. TM-bus, control-bus
  4. modules
  5. FPGA design compatibility
  6. module configuration
- **System-selftest must not fail, to put interlock system into operation mode**

Saved Systest output at startup(1238 Bytes)

```
ID-Signature of station #0:
INTLK3_CNTRL_M Rev.: C142      Powerups:0      Serial: 0000:0000:0000:0000
-----
[ Board-Test-#0] : passed
[ ICS-Test-#0]  : passed

ID-Signature of station #2:
INTLK3_WINC_V Rev.: B456      Powerups:88     Serial: 0000:0000:FFFF:FFFF
-----
[CntrlBus-Test-#2] : passed
[ SRQ-Test-#2]   : passed
[ TM-Bus-Test-#2] : passed
[ ICS-Test-#2]   ERROR: station is a untested virgin module!

ID-Signature of station #3:
INTLK3_WINC_V Rev.: B456      Powerups:88     Serial: 0000:0000:FFFF:FFFF
-----
[CntrlBus-Test-#3] : passed
[ SRQ-Test-#3]   : passed
[ TM-Bus-Test-#3] : passed
[ ICS-Test-#3]   ERROR: station is a untested virgin module!

ID-Signature of station #5:
INTLK3_DIGIIO Rev.: C123      Powerups:0      Serial: 0000:0000:0000:0000
-----
[CntrlBus-Test-#5] : passed
[ SRQ-Test-#5]   : passed
[ TM-Bus-Test-#5] : passed
[ ICS-Test-#5]   ERROR: station is a untested virgin module!

System Test finished.
Error = 1
Systest FAILED !
```



# Interlock HTTP Interface

- display actual signal states
- edit signal-masks
- edit interlock configuration

Sig.	Used ( <input checked="" type="checkbox"/> )	Name	Threshold	Off Action	Type
1	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Transformer Tank	F < Fmin	Modulator off Bias PS off	mech. Contact (pot. free)
2	<input type="checkbox"/> <input type="button" value="Set"/>	Flow Klystron Collector	F < Fmin	Modulator off	mech. Contact (pot. free)
3	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Klystron Body	F < Fmin	Modulator off	mech. Contact (pot. free)
4	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Solenoid 1..3	F < Fmin		
5	<input type="checkbox"/> <input type="button" value="Set"/>	Flow Modulator	F < Fmin		
6	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow PreAmp	F < Fmin		

1	2	3	4	5	6	7
11	12	13	14	15	16	17
21	22	23	24	25	26	27
31	32	33	34	35	36	37
41	42	43	44	45	46	47
51	52	53	54	55	56	57
61	62	63	64	65	66	67
71	72	73	74	75	36	37
81	82	83	84	85	86	87
91	92	93	94	95	96	97
101	102	103	104	105	106	107
111	112	113	114	115	116	117
121	122	123	124	125	126	127
131	132	133	134	135	136	137
141	142	143	144	145	146	147
151	152	153	154	155	156	157

### INTLK3 Status

Views: [Standard View](#) [Alternate View](#) [View All](#) [Overview \(matrix\)](#) [Refresh](#)

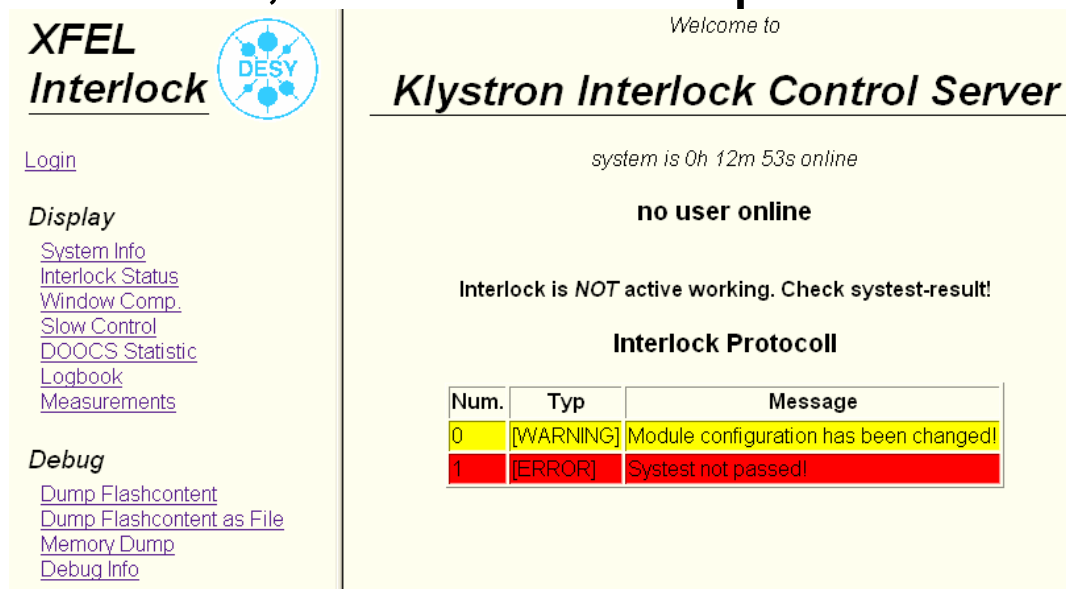
STATMASK Config was **changed** - [store config](#) or - [rewind config](#)

FlowBox

Sig.	Used ( <input checked="" type="checkbox"/> )	Name	Threshold
1	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Transformer Tank	F < Fmin
2	<input type="checkbox"/> <input type="button" value="Set"/>	Flow Klystron Collector	F < Fmin
3	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Klystron Body	F < Fmin
4	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Solenoid 1..3	F < Fmin
5	<input type="checkbox"/> <input type="button" value="Set"/>	Flow Modulator	F < Fmin
6	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow PreAmp	F < Fmin
9	<input checked="" type="checkbox"/> <input type="button" value="Set"/>	Flow Circulator 1	F < Fmin

# Interlock HTTP Interface

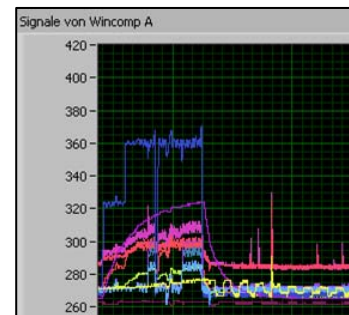
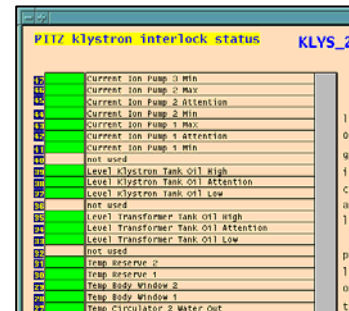
- server runs on the controller (*NIOS/II processor*)
- web-interface, access via browser
- user authentication
- Different User Roles (*chief engineer, engineer, technician*)
- IP-Address check, 2 addresses possible



The screenshot shows the XFEL Interlock web interface. On the left is a navigation menu with links for Login, Display (System Info, Interlock Status, Window Comp., Slow Control, DOOCS Statistic, Logbook, Measurements), and Debug (Dump Flashcontent, Dump Flashcontent as File, Memory Dump, Debug Info). The main content area displays 'Welcome to Klystron Interlock Control Server', 'system is 0h 12m 53s online', and 'no user online'. A warning message states 'Interlock is NOT active working. Check systest-result!'. Below this is an 'Interlock Protocoll' table with two entries: a warning about module configuration changes and an error about the system test failing.

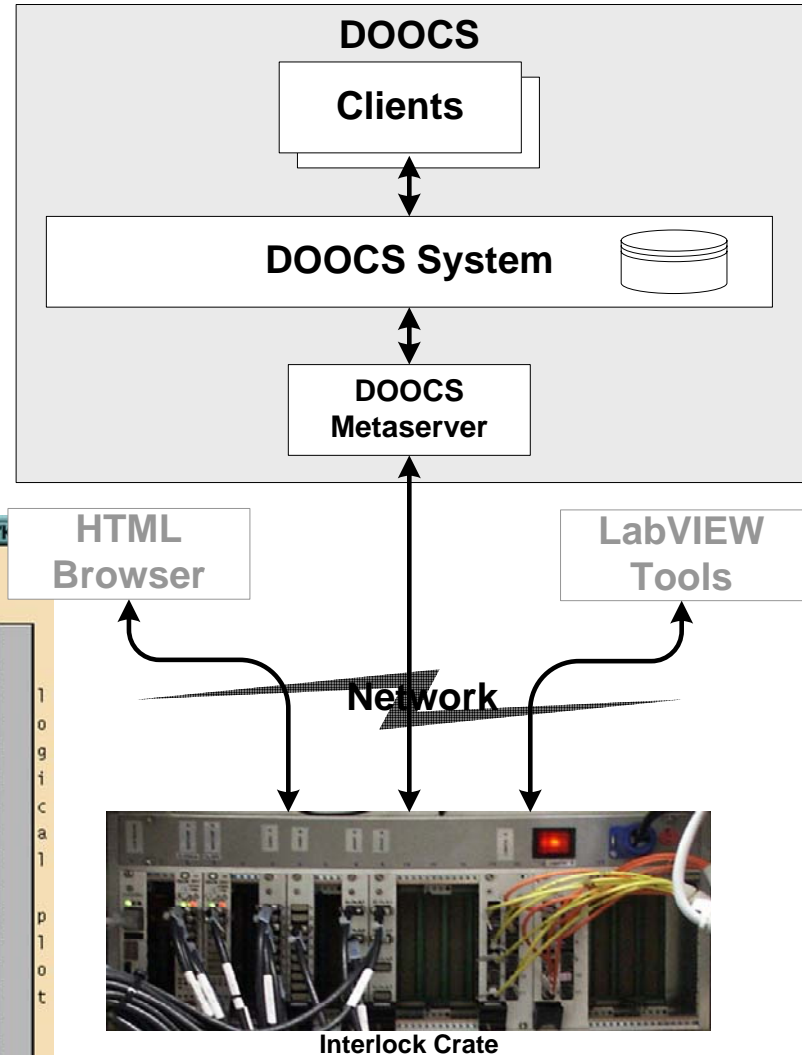
Num.	Typ	Message
0	[WARNING]	Module configuration has been changed!
1	[ERROR]	Systest not passed!

- DOOCS Interface for viewing state
  - Integration into the control-system
  
- Tools under LabVIEW
  - Detailed error diagnostics



# Interlock to DOOCS - Interface

- Interlock sends actual status data to Metaserver
- Metaserver integrates status-data into DOOCS-System and history
- Clients monitor signal states



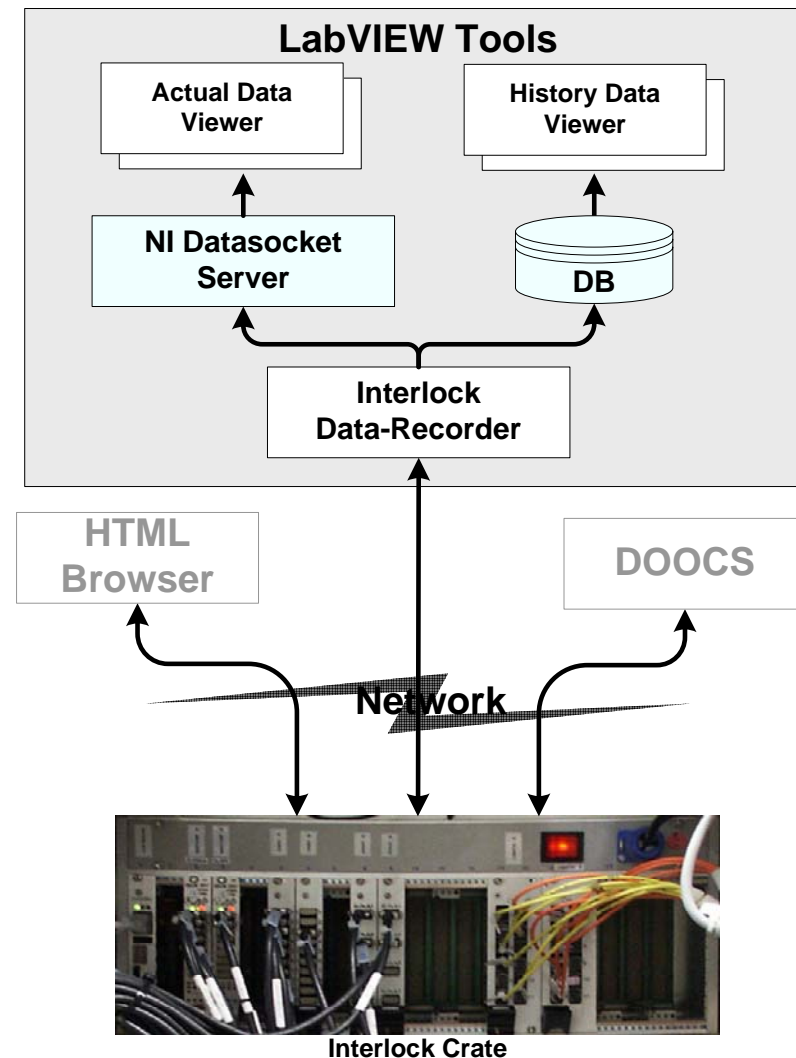
pitiz\_interlock\_klystron: PITZ.I\_LOCK/KLYS/

PITZ klystron interlock status      KLYS\_2 / RF2 -> booster

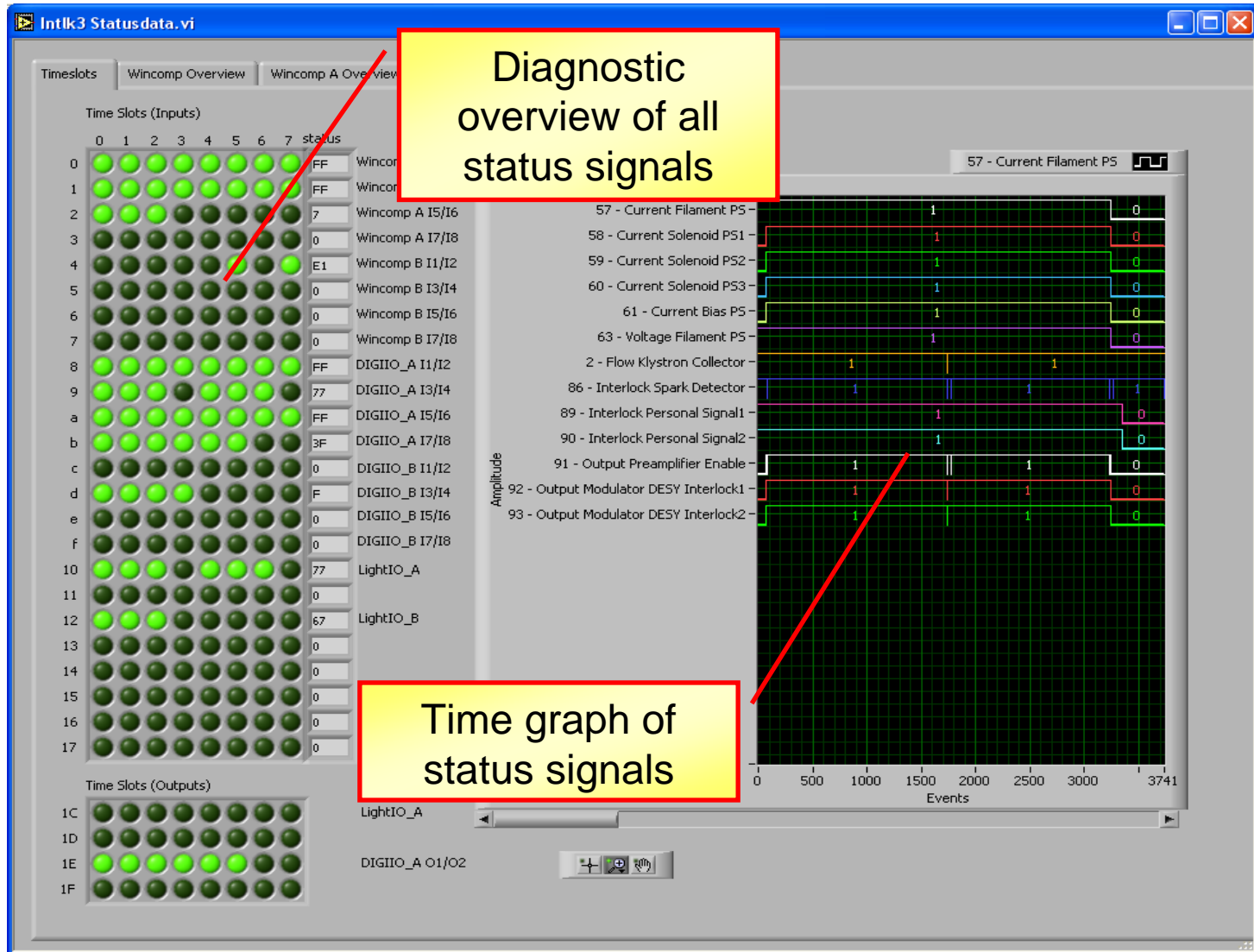
47	Current Ion Pump 3 Min	95	not used
46	Current Ion Pump 2 Max	94	not used
45	Current Ion Pump 2 Attention	93	not used
44	Current Ion Pump 2 Min	92	not used
43	Current Ion Pump 1 Max	91	Output Preamplifier Enable
42	Current Ion Pump 1 Attention	90	Interlock Personal Signal2
41	Current Ion Pump 1 Min	89	Interlock Personal Signal1
40	not used	88	Clock Input Bouncer
39	Level Klystron Tank Oil High	87	Interlock RF Leakage Detector
38	Level Klystron Tank Oil Attention	86	Interlock Spark Detector
37	Level Klystron Tank Oil Low	85	Status Preamplifier Ready
36	not used	84	not used
35	Level Transformer Tank Oil High	83	not used
34	Level Transformer Tank Oil Attention	82	not used
33	Level Transformer Tank Oil Low	81	not used
32	not used	80	not used
31	Temp Reserve 2	79	not used
30	Temp Reserve 1	78	Power Gun Pwrmeter W02 Reflected Max
29	Temp Body Window 2	77	Power Gun Pwrmeter W01 Reflected Max
28	Temp Body Window 1	76	Power Circulator Pwrmeter W02 Reflected Max
27	Temp Circulator 2 Water Out	75	Power Circulator Pwrmeter W01 Reflected Max
26	Temp Circulator 1 Water Out	74	Power Klystron Pwrmeter W02 Reflected Max
25	Temp Dummy Load 2 Water Out	73	Power Klystron Pwrmeter W01 Reflected Max

# Interlock to LabVIEW - Interface

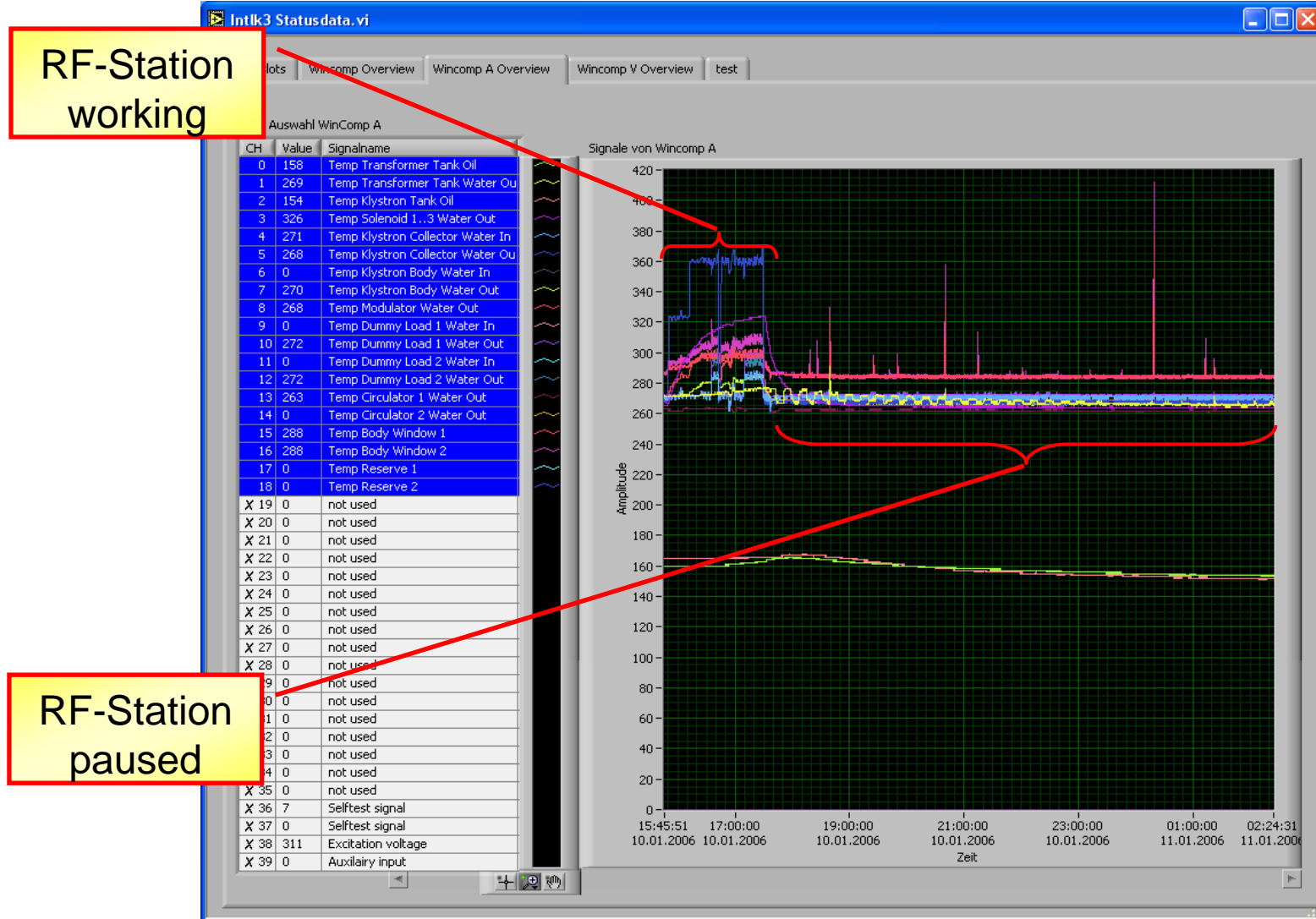
- used for diagnostic
- view detailed information about interlock signals
- store highly detailed data into database for later diagnostic
- very helpful on resolving errors



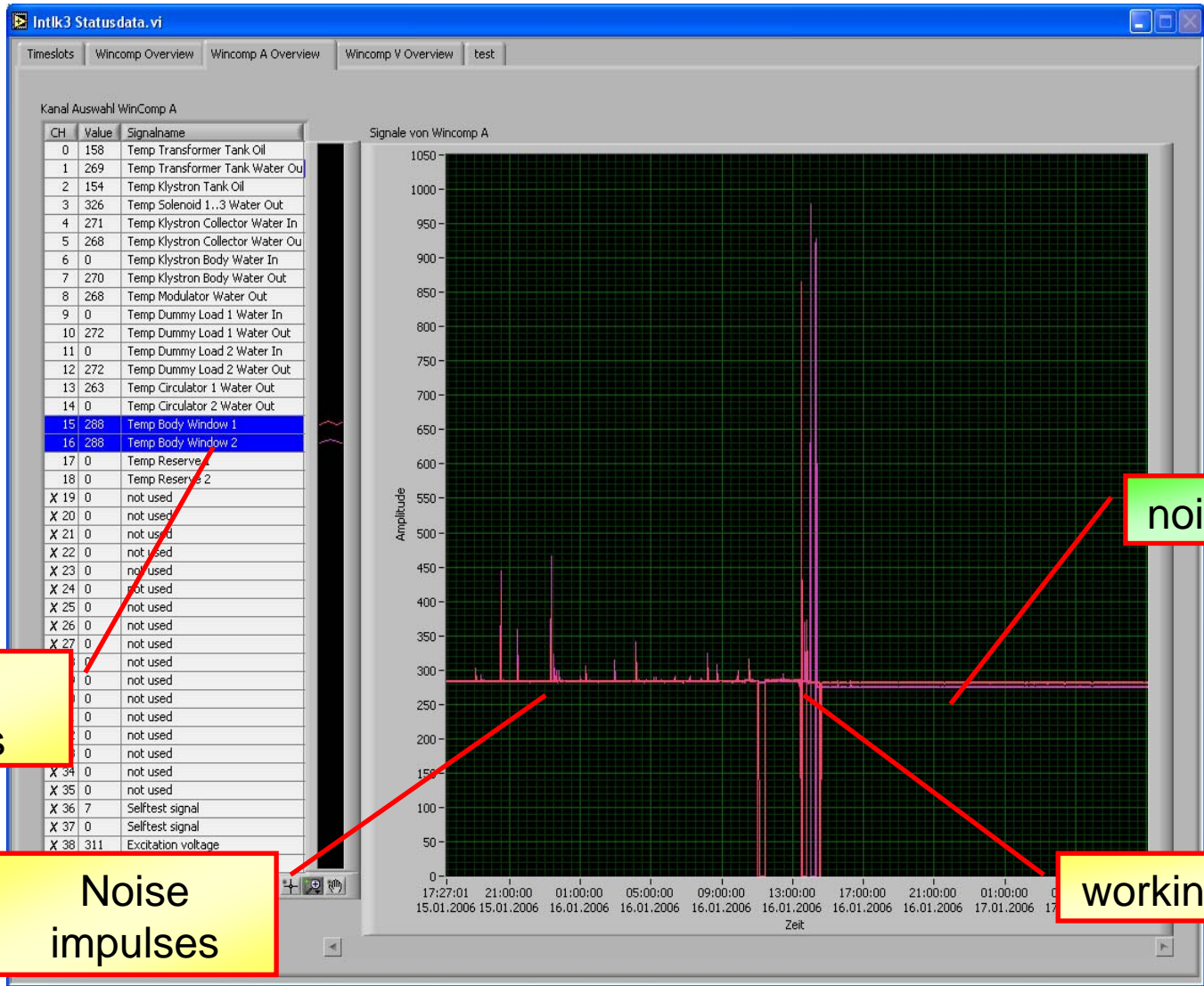
# Diagnostic with LabVIEW



# Viewing Timegraph Curves



# Example: Help with cable diagnose



Select Curves

Noise impulses

noise removed

working on cables





- Highly flexible Interlock System for XFEL
- Interlock-function implemented in hardware
- Process many signals with different types
- Signals can be masked
- Updateable firmware over intranet
- High connectivity to other applications
  - DOOCS, LabVIEW, HTML-Browser

**Thank you for your attention!**

